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Characterisation and Integration of Materials and Processes for Planar Spiral Microinductors with Permalloy Cores

Ross Walker

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Abstract

The increasing density of electronics within portable electronic devices provides the motivation to develop more compact power electronics, such as DC-DC converters. Typically, integrated circuits and each passive component, such as inductors, are discreetly packaged and mounted on printed circuit board (PCB), to implement the converter. Hence for further size reduction there has been growing interest for integration schemes such as Power supply in package (PwrSiP). However, the ultimate goal is the monolithic integration of the power supply solution, in an integration scheme known as Power Supply on Chip (PwrSoC).

The economic effectiveness of the converter will be determined by the device footprint and number of processing steps required to fabricate the inductor. Hence, the motivation behind this thesis is the need for microinductors with large inductance density (inductance per device footprint) while maintaining low losses, which can be integrated with silicon IC. Furthermore, the need for thick layers will result in issues with yield and reliability of the fabricated device. Hence there is a need to identify, characterise and integrate materials with low residual stress into the microinductor fabrication process.

A typical choice of inter-coil dielectric is the photo-definable epoxy SU-8. However, SU-8 suffers from intrinsic issues with high residual stress and adhesion. One possible replacement for SU-8 as a structural and dielectric layer is Parylene-C. The first objective of this thesis proposes a test-bed inductor process, which incorporates Parylene as a structural and dielectric layer and has a short turnaround time of one week. This fabrication process involves the filling of high aspect ratio gaps between copper structures with Parylene and subsequent chemical mechanical planarisation, and a test chip has been designed to characterise these processes. Additionally, Scotch-tape testing has been used to confirm suitable Parylene adhesion to patterned and unpatterned films used in this process. Subsequently, complete microinductors, with magnetic cores, have been fabricated, characterised and benchmarked against other inductor technologies and architectures reported in the literature.

Parylene is expected to produce films with low residual stress due to its room

temperature deposition process. However, the test-bed inductor process requires thermal treatments up to 140°C. Hence it was necessary to characterise the stress in Parylene films as a result of processing temperature and compare this to stress levels in SU-8 5 and 3005 films. This study has determined the spatial variation of residual stress in Parylene-C and SU-8 films, by combining automated measurements of strain indicator test structures and local nanoindentation measurements of Young's modulus. These measurements have been used to wafer map strain, Young's modulus, and subsequently residual stress in these films, as a result of processing parameter variation.

It is well known that placing ferromagnetic material in close proximity to current carrying coils can further enhance the measured inductance value. However, the conductive magnetic core is also a source of loss for the microinductor. Hence, magnetic permeability, electrical resistivity and mechanical stress in the magnetic core influence the inductance value, eddy current losses and reliability of the fabricated microinductor, respectively. The ability to characterise these properties on wafer is essential for process control and verification measurements. This thesis details a test chip capable of routine measurements on NiFe films to characterise the spatial variation of these properties. Furthermore, wafer mapping measurements are reported to identify the correlation between high frequency permeability, electrical resistivity, mechanical strain and the chemical composition of two-component Permalloy film ($Ni_xFe_{(100-x)}$) electroplated on the surface of 100mm silicon wafers.

Finally, MEMS-based inductor fabrication processes typically require a number of electrodeposition steps, which require conductive seed layers for the deposition of the coils and magnetic core material. A typical choice of seed layer is copper. However, due to copper's paramagnetic behaviour ($\mu = 1$) and low electrical resistivity (ρ=6.69$\mu\Omega$.cm) this layer contributes to eddy current losses, while acting as a thin 'screening layer'. It is very likely that using a magnetic seed layer, within the magnetic core, will noticeably reduce eddy current related losses. However, detailed systematic experimental studies on any such improvement have not been documented in the literature. This study involves compositional, structural, electrical and magnetic characterisation of $Ni_{80}Fe_{20}$ films electro-deposited on non-magnetic and magnetic

seed layers (i.e. copper and nickel respectively). Mechanical strain test structures and X-ray analysis have been used to characterise the stress levels and structural properties of $Ni_{80}Fe_{20}$ films electro-deposited on both copper and nickel seed layers. In addition, planar spiral micro-inductors, both with and without patterned magnetic cores, have been fabricated to determine the effect of patterning on their performance. This is in addition to quantifying the improvement in the electrical performance resulting from the enhanced magnetic and resistive contribution provided by magnetic seed layers.

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Declaration

The candidate confirms that the work submitted is his own, except where work which has formed part of jointly-authored publications has been included. The contribution of the candidate and the other authors to this work has been explicitly indicated below. The candidate confirms that appropriate credit has been given within the thesis where reference has been made to the work of others.

The candidate hereby declares that the work has not been submitted for any other degree or professional qualification.

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Acronyms and Abbreviations

AFM	Atomic Force Microscope
Au	Gold
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
Cu	Copper
CVD	Chemical Vapour Deposition
DC	Direct Current
FIB	Focused Ion Beam
HF	Hydrofluoric Acid
IC	Integrated Circuit
MEMS	MicroElectroMechanical Systems
Ni	Nickel
NiFe	Nickel Iron
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
Si	Silicon
Ti	Titanium
UV	Ultra Violet
XRF	X-ray Fluorescence
XRD	X-ray Diffraction

List of Publications

The following papers were prepared in the development of this thesis:

1. R. Walker, E. Sirotkin, J.G. Terry, S. Smith, A.J. Walton, "Characterisation and Integration of Parylene as an Insulating Structural Layer for High Aspect Ratio Electroplated Copper Coils," *2013 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Osaka, Japan, March 2013, pp. 7-12.

2. R. Walker, E. Sirotkin, J.G. Terry, S. Smith, M.P.Y. Desmulliez, A.J. Walton, "Effect of Seed Layer on the Performance of Planar Spiral Microinductors," *2014 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Udine, Italy, March 2014, pp. 135-140.

3. R. Walker, E. Sirotkin, J.G. Terry, S. Smith, M.P.Y. Desmulliez, A.J. Walton, "Characterisation of Stress in Dielectric Films by Automated Wafer Mapping," *2014 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Udine, Italy, March 2014, pp. 98-103.

4. E. Sirotkin, R. Walker, J.G. Terry, S. Smith, A.J. Walton, "Air-CPW test structure for broadband permeability spectra measurements of thin ferromagnetic films," *2014 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Udine, Italy, March 2014, pp. 177-181.

5. E. Sirotkin, S. Smith, R. Walker, J.G. Terry, A.J. Walton, "Test Structures for the Wafer Mapping and Correlation of Electrical, Mechanical and High Frequency Magnetic Properties of Electroplated Ferromagnetic Alloy Films," *2015 IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Phoenix, USA March 2015, pp.183-187.

Chapter 1
Introduction

1.1 Introduction

In 1965 Gordon Moore predicted that the number of transistors per square inch would double every eighteen months to two years. This trend has since been known as Moore's law, and its continuation has become a primary goal of the semiconductor industry [1, 2]. However, the trend in size reduction of passive components, such as inductors, has not reached the same level as transistors. Furthermore, the increasing number of portable electronic devices and density of electronics within these devices has resulted in the need for more compact power electronics, such as DC-DC converters [3, 4]. An example of an inductive switching DC-DC converter schematic is presented in figure 1.1.

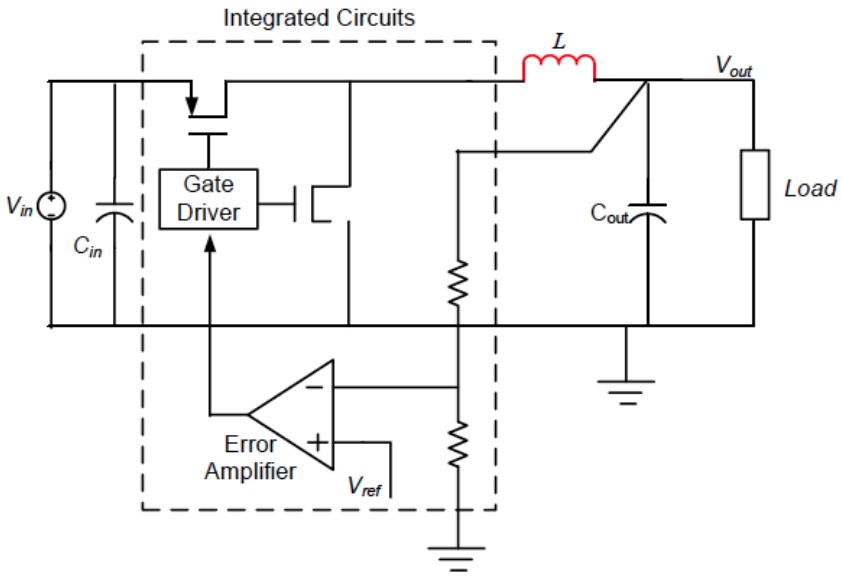


Figure 1.1: *Schematic diagram of inductive switching DC-DC converter [5].*

In the case of the converter presented in figure 1.1, it would be typical for the integrated circuit, inductor and capacitors to be packaged discreetly and implemented on printed circuit board (PCB). Recently interest has been growing for integration schemes such as Power Supply in Package (PwrSiP). With this integration method, the passive components would be packaged together, separately from the integrated circuit. However, the ultimate goal is the monolithic integration of the power supply

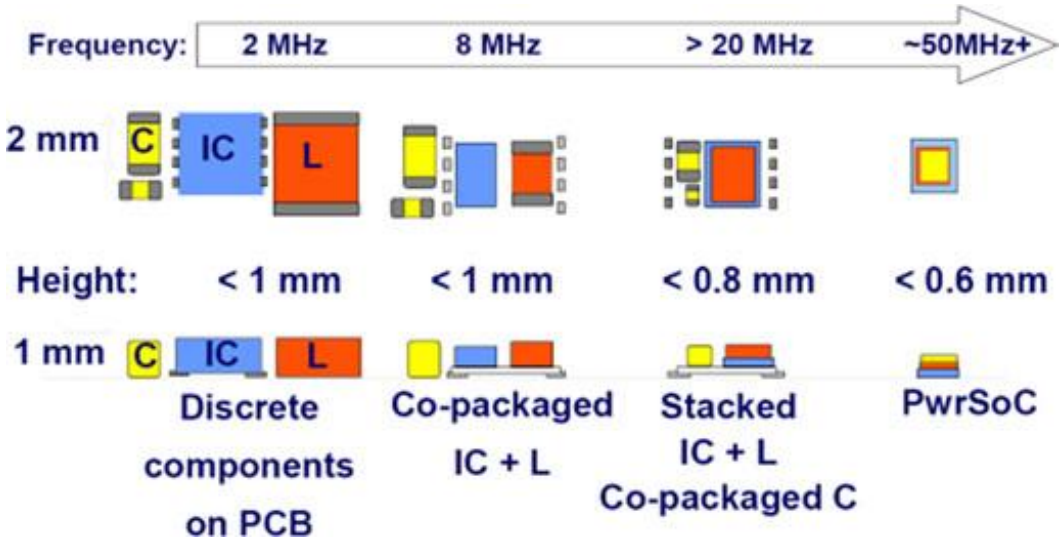


Figure 1.2: *Expected progression from discreet components mounted on PCB to PwrSoC [4].*

solution, in an integration scheme known as Power Supply on Chip (PwrSoC) [6, 7]. Figure 1.2 presents the expected progression of the power supply solution from discreet components mounted on PCB to PwrSoC [4].

The advantages of the PwrSiP and PwrSoC schemes for device footprint (area occupied by the device) reduction and space-limited applications are obvious. However, these schemes are also attractive as they allow for reduced inventory and assembly costs. Furthermore, from the consumer's perspective they provide more reliable, compact and economical devices [3].

Typically, the inductor will consume the majority of the area occupied by the converter. For example Wens [8] developed a converter with footprint 1.6mm × 2.35mm where the combined footprint of the four integrated inductors measured 2mm × 2mm [4]. The economic effectiveness of the converter will be determined by the device footprint and number of processing steps required to fabricate the inductor [9]. Hence, the motivation behind this thesis is the need for microinductors with large inductance density (inductance per device footprint) while maintaining low losses, which can be integrated with silicon IC. Additionally, Mathu [4] reported that following integration the height of the power supply solution would be maintained in the range of hundreds of micrometres. This need for thick layers will result in issues with reliability and yield of the fabricated device. Hence, there is a need to identify,

characterise and integrate materials with low residual stress into the microinductor fabrication process.

1.2 Research Aims

An inductor is a device that produces a voltage as a result of a time varying current. Hence, inductors are often thought of as devices which store energy in the magnetic field, produced by this time varying current. Winding the conductor to form a coil intensifies the magnetic field and results in greater inductance values. Furthermore, placing ferromagnetic material in close proximity to the coils can further enhance inductance values. From the definition that inductors store energy in a magnetic field, the use of ferromagnetic material to enhance the inductance values is intuitive.

Typically power inductors realised by MEMS technology are described by one of two architectures. These are the spiral and solenoid/toroidal microinductors, and images of these inductors and their cross-sections are presented in figure 1.3 (a) and (b), respectively. As is clear from this figure, spiral inductors have the magnetic core 'wrapped around' the coils, whereas for the solenoid architecture the coils are wrapped around the magnetic core. Planar spiral inductors are possibly the most widely reported microinductors and have been reported to produce, high quality (Q)-factor; inductance per device area; and low DC resistance [4, 10, 11], for this reason these inductors have been studied in this thesis.

In 1979 Soohoo [12] proposed a model, which detailed that the inductance value of a solenoid inductor increases proportionally with the relative permeability of its magnetic core. Hence, the effective implementation of the magnetic core will result in a reduced number of turns, and area, occupied by the device required to achieve a desired inductance value [13]. However, in practise achieving higher inductance values requires inductors to be fabricated with more turns and/or a greater volume fraction of magnetic material. This results in resistive losses in the coil and core, and magnetic losses in the core. Hence, it is typical for efficiency to be sacrificed at the expense of increasing the value of the inductance. The efficiency of the inductor is characterised by its Q-factor, which is defined as the ratio of energy stored to energy lost per cycle. Therefore, typically inductance can be increased at the expense of Q-factor.

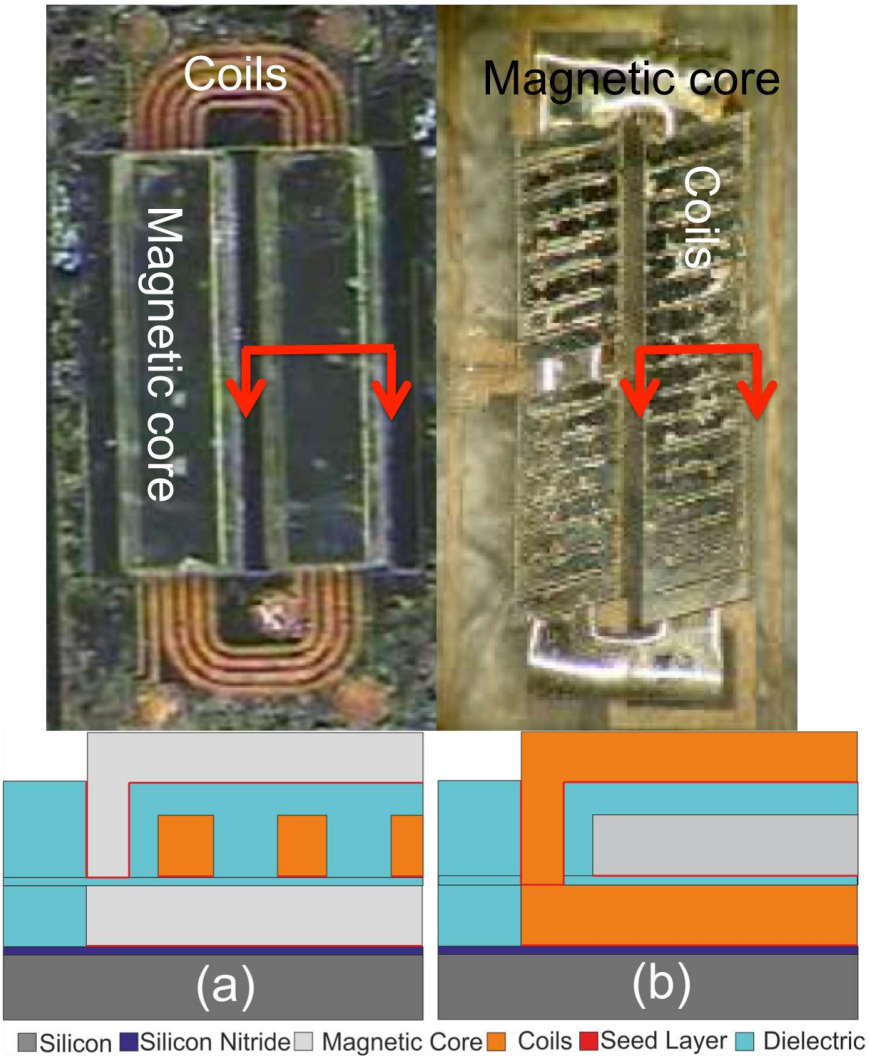


Figure 1.3: *Top down view and cross-section of (a) planar spiral and (b) toroidal microinductor [14, 15].*

1.3 Effect of Seed Layer and Patterned Magnetic Cores on the Performance of Microinductors

The electrodeposition of magnetic layers requires the use of a conductive seed layer. One source of losses in the magnetic core, which has been overlooked until recently, arises from the use of copper as a seed layer. As a result of copper's low electrical resistivity and paramagnetic behaviour these seed layers contribute to eddy current losses while acting as a thin 'screening layer'. This screening effect results from the eddy current formation in the seed layer, which creates an opposing magnetic field to that produced by the inductor coils. It is postulated that the use of a magnetic seed layer should improve performance and efficiency of the inductor. However, detailed

systematic experimental studies on any such improvement have not been documented in the literature.

Additionally, the microinductor presented in figure 1.3 (a) has an unpatterned and non-laminated core. Hence, losses in the core will be incurred as a result of electric currents, known as eddy currents, which will form in the conductive core as a result of the time varying magnetic field produced by the coils. In order to reduce eddy currents in the core, it is typical to disrupt the current path by patterning the magnetic core. Examples of inductors with patterned magnetic cores are presented in figure 1.4.

It will be an aim of this thesis to characterise the effect of seed layer on the performance of planar spiral microinductors with a number of different patterned magnetic cores.

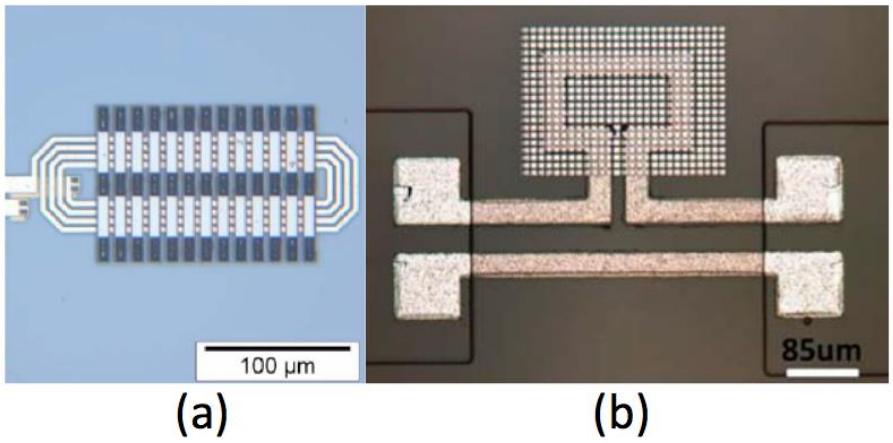


Figure 1.4: *Examples of planar spiral microinductors with (a) laminations perpendicular to the coils, and (b) mesa structure patterned cores [16, 17].*

1.4 Dielectric Layers

The requirement for power inductors to pass large currents, results in the need for thick coils, and subsequently thick dielectric layers. An attractive and typical choice for these dielectric layers is the photo-definable epoxy SU-8 [15, 18-31]. SU-8 is used in many MEMS applications due to its high thermal and chemical stability and ability to achieve 2mm thick layers from single deposition, where 40:1 aspect ratios have been achieved [32, 33]. The attraction of SU-8 for microinductor applications is that it can be used to form the mould for electroplating, and then be left in the structure to form the inter-coil dielectric and structural layer. Hence, there is no need for additional

processes for gap filling between the high aspect ratio coils. However, SU-8 suffers from issues with high residual stress and delamination, which creates issues with reliability and yield of the fabricated inductors. Hence, there is clearly a need to determine a suitable material to replace SU-8 and integrate this with a microinductor fabrication process.

One possible alternative to SU-8 is that of Parylene-C. This room temperature chemical vapour deposited (CVD) polymer, is currently used as a protective coating for printed circuit boards. However, its conformal, low temperature and intrinsic low stress deposition process make it a promising alternative to SU-8 [34, 35].

An inductor fabrication process that incorporates Parylene offers challenges, such as ensuring suitable gap filling performance between high aspect ratio trenches; adhesion with other materials used in the inductor fabrication process; and compliance with processes, such as chemical mechanical polishing (CMP).

Additionally, reducing residual stress in deposited films is one of the main challenges for the improvement of yield and reliability of the inductor device. It is important to characterise the residual stress in the Parylene film and compare it with that of SU-8.

1.5 Test Structures

Test structures, which have been specifically designed for material characterisation and process optimisation, have been in use since the early 1960s. The attraction of using test structures is that they can be fabricated with a short turnaround time, and can often be integrated with the device fabrication process to confirm wafers have been processed successfully [36].

In the case of microinductors, magnetic permeability; electrical resistivity; and residual mechanical stress properties of the electroplated NiFe core directly influence the inductance; resistive core losses; and mechanical reliability of the fabricated device. A test chip that allows for the on wafer characterisation of all of these properties supports the optimisation of magnetic film properties. Test structures have been reported in literature that characterise mechanical stress and electrical resistivity [16, 37-39] in magnetic materials. However, test structures capable of the routine measurement of permeability using standard electrical probing have not been previously reported. It will be an aim of this thesis to develop a test chip capable of

routine measurements to characterise these properties. Furthermore, this test chip will be used to characterise and correlate the compositional, dimensional, electrical, mechanical and magnetic properties.

Additionally, test structures will be employed in this thesis to characterise residual stress in dielectric layers; inter-coil dielectric fill performance and planarisation.

1.6 Summary

To summarise, the following research objectives are addressed in this thesis:

- Develop a test-bed inductor process with short fabrication time, which will allow for the fast characterisation of new materials and processes with regards to the inductor fabrication process and device performance.
- Characterise the performance of Parylene-C when integrated into the planar spiral inductor process, as an alternative to SU-8 dielectric and structural layers.
- Characterise the residual stress in Parylene-C and compare this with SU-8.
- Develop a test chip with the ability to characterise the electrical, mechanical and magnetic properties of the electroplated core and determine the spatial variation and correlation between these properties through automated wafer mapping.
- Characterise the effect of seed layer on the properties of electrodeposited NiFe and subsequently the effect on the performance of planar spiral microinductors with a number of different patterned magnetic cores.

1.7 Thesis Plan

Chapter 2: Background

This chapter reports on the characterisation of inductor performance and losses. An example of a planar spiral microinductor process developed by National Semiconductor is presented in this chapter. This fabrication process includes the use of SU-8 as a dielectric and structural layer, as well as electroplated copper and NiFe for coils and magnetic core, respectively. The use of these processes has been characterised based upon that reported in literature, and technological challenges have

been highlighted. Finally, inductors reported in literature have been benchmarked to define the current state of the art.

Chapter 3: Characterisation and Integration of Parylene as an Insulating Structural Layer for High Aspect Ratio Electroplated Copper Coils.

This chapter reports the development of processing methods and test structures for the characterisation and evaluation of Parylene-C as an insulating structural layer material for integration with planar microinductors. The process involves the filling of high aspect ratio gaps between copper structures with Parylene and subsequent chemical mechanical planarisation. A test chip has been designed to characterise this process and the results are presented. Subsequently complete microinductors, with magnetic cores, have been fabricated, using the test bed microinductor process, to demonstrate the capability of the process.

Chapter 4: Characterisation of Residual Stress in Dielectric Films Studied by Automated Wafer Mapping.

SU-8 develops high levels of stress during processing. This chapter reports detailed quantitative data following previous work presented in chapter 3, where Parylene-C has been proposed as a possible replacement for SU-8. In particular, this chapter details the characterisation of residual stress in (i) SU-8 films as a function of processing temperatures and (ii) post-processing thermally treated Parylene-C. This characterisation includes wafer-mapping strain using rotating pointer arm test structures, and deriving the stress from independent measurements of strain and Young's modulus.

Chapter 5: Test Structures for the Wafer Mapping and Correlation of Electrical, Mechanical, High Frequency Magnetic, and Composition of Electroplated Ferromagnetic Alloys.

This chapter presents a method of measuring the permeability of patterned electroplated structures and brings together the simultaneous wafer mapping of magnetic permeability, electrical resistivity and mechanical strain of electroplated ferromagnetic films together with the thickness of the films and their composition. The wafer mapping of all these properties using simple automated electrical and optical measurements facilitates the spatial correlation between different parameters taking into account film thickness variations over the wafer. This enables the uniformity of

the electrodeposited NiFe to be analysed and supports the optimisation of film properties.

Chapter 6: Effect of Seed Layer on the Performance of Planar Spiral Microinductors.

This chapter reports on the effect of the electrical performance related to magnetic seed layers used within planar power microinductors. These studies involve structural and magnetic characterisation of $Ni_{80}Fe_{20}$ films electro-deposited on non-magnetic and magnetic seed layers (i.e. copper and nickel respectively). Microelectronic mechanical test structures and X-ray analysis have been used to characterise the stress levels and structural properties of $Ni_{80}Fe_{20}$ films electro-deposited on both copper and nickel seed layers. In addition, planar spiral micro-inductors, with patterned magnetic cores, have been fabricated in order to confirm the improvement in the electrical performance from magnetic seed layers, as a result of enhanced magnetic and resistive contribution.

Chapter 7: Conclusions and Future Work

This chapter reviews the achievements and results presented in this thesis and highlights conclusions based upon conducted experimental work. Additionally, this chapter highlights the impact of the presented research and outlines suggested future work.

Appendices

Fabrication process run sheets, enlarged wafer maps and experimental data relating to this thesis.

Chapter 2
Background

2.1 Introduction

The purpose of this chapter is to review that which has already been published in the field of microinductor technology. This chapter characterises parameters used to define the performance, efficiency, and loss mechanisms in planar spiral microinductors. Additionally, a planar spiral inductor fabrication process, developed by National Semiconductor, will be presented. This fabrication process involves a number of materials and processing steps, which are typical of microinductor fabrication processes reported in literature. Work reported in literature to characterise these materials and processes will be presented in this chapter, and attention will be drawn to technological challenges. Finally, inductors reported in literature will be benchmarked to define the current state of the art.

2.2 Inductor Characterisation

2.2.1 Inductance

Inductance is a measure of the voltage induced in a conductor (self-inductance) and nearby conductors (mutual inductance) when a time varying current is passed though the conductor. Inductance is measured in Henrys (H), and it follows that one Henry is achieved when a current change of one ampere per second results in a voltage of 1 volt [40, 41].

Inductance arises from the production of a magnetic field as a result of a time varying current in a conductor, and the voltage induced in a conductor as a result of the produced magnetic field. Hence, inductance arises from the application of both Ampere's and Faraday's law. For a single turn winding excited by a time varying current $(i(t))$, as presented in figure 2.1 (a), the induced magnetic field follows Ampere's law:

$$i(t) = \oint H(t)dl \tag{2.1}$$

where $H(t)$ is the instantaneous magnetic field strength, and dl is the magnetic flux path length.

When a time varying magnetic flux passes through a conductive loop, as presented in figure 2.1 (b), a voltage is induced across the terminals of the conductive loop. The instantaneous magnitude of voltage produced ($v(t)$) is related to the rate of change of magnetic flux (Φ) flowing through the loop, and follows Faraday's law:

$$v(t) = -\frac{\mathrm{d}\Phi(t)}{dt} = -A_C \frac{dB(t)}{dt} \tag{2.2}$$

where, A_C is the area occupied by the loop and $B(t)$ is the instantaneous magnetic flux density.

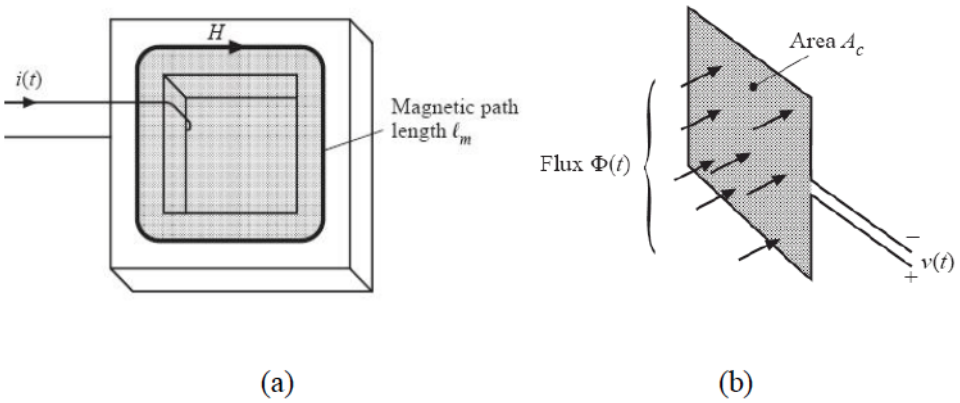


Figure 2.1: *Illustrations of (a) Single turn conduction loop and toroid core; (b) single turn conduction loop with magnetic flux passing through the cross-section [42].*

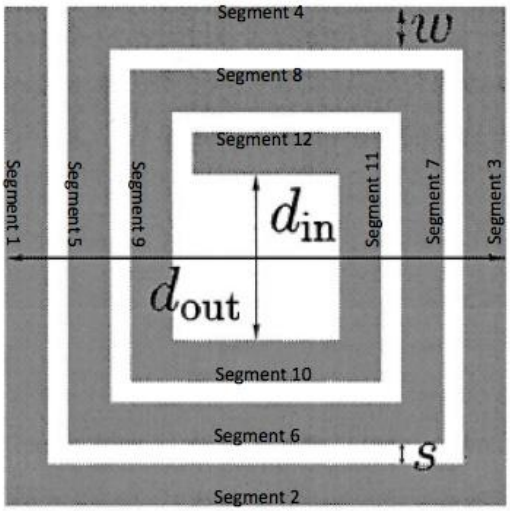


Figure 2.2: *Schematic diagram of an inductor coil [43].*

When the conductor is made into a loop, as in figure 2.1 (b), the magnetic field at the centre of the loop intensifies, and hence the conductor's inductance value increases. Fabricating the conductor to form a spiral coil, as presented in figure 2.2 results in further improvement of the inductance value. These spiral coils can be considered as a number of segments. For example, the three-turn inductor presented in figure 2.2 consists of 12 segments, where d_{in} and d_{out} equal the dimensions of the coils internal and external diameters, respectively [43]. The total inductance of the coil is determined by summing the self-inductance (L_S) of each segment and the mutual inductance (L_M) experienced between each segment:

$$L_T = \sum L_s + \sum L_M \tag{2.3}$$

Self-inductance is defined as the voltage induced in the conductor as a result of its own time varying magnetic field, and for a straight conductor the self-inductance is given by [44]:

$$L = 2l\left\{\ln\left(\frac{2l}{w+t}\right) + 0.50049 + \frac{(w+t)}{3l}\right\} \tag{2.4}$$

Mutual inductance is defined as voltage induced in conductors parallel to the conductor of interest. For example, in the three-turn inductor presented in figure 2.2, mutual inductance will arise between segment 1 and segments 3,5,7,9, and 11. Mutual inductance between segment i and j is given by:

$$L_{i,j} = 2l\left(\ln\left(\left(\frac{l}{GMD}\right) + \left[1 + \left(\frac{l^2}{GMD^2}\right)\right]^{\frac{1}{2}}\right) - \left[1 + \left(\frac{GMD^2}{l^2}\right)\right]^{\frac{1}{2}} + \left(\frac{GMD}{l}\right)\right) \tag{2.5}$$

where l is the length of the shortest segment and GMD is the geometric mean distance. GMD can be approximated as the pitch of the filaments. However, an exact value of GMD may be calculated from:

$$\ln GMD_{i,j} = \ln d - \left\{\left[\frac{1}{12\left(\frac{d}{w}\right)^2}\right] + \left[\frac{1}{60\left(\frac{d}{w}\right)^4}\right] + \left[\frac{1}{360\left(\frac{d}{w}\right)^8}\right] + \left[\frac{1}{660\left(\frac{d}{w}\right)^{10}}\right]\right\} \tag{2.6}$$

where t, d and w are the segment thickness distance between segment centres and width respectively.

For solenoid inductors, the inductance is often approximated by the Soohoo model[12, 45]:

$$L = \frac{\mu n^2 w t}{l} \tag{2.7}$$

where μ, n, w, t and l are the permeability, number of turns, width, thickness and length of the magnetic core respectively. It has been widely reported that equation 2.7 is oversimplified and does not take into account any loss mechanisms. Hence, calculated inductance values are typically orders of magnitude overestimations. However, this equation highlights the importance of permeability on the actual inductance value. This equation reports on the absolute permeability(μ), where $\mu = \mu_o \mu_r$, and μ_o is the permeability of free space ($4\pi \times 10^{-7}$) H·m^{-1}. Permeability is not a property of the material, rather a ratio of the magnetic flux density in a material to a given applied field. Hence, it can be thought of as a measure of how easily a material is magnetised. The relative permeability (μ_r) is dependant upon a number of factors, such as material properties; layer geometry; process conditions and external testing parameters. Typically for non-ferromagnetic materials, such as air, dielectrics, and non-magnetic metals the relative permeability (μ_r) is 1. However, for ferromagnetic materials, such as iron, cobalt, nickel and their alloys relative permeabilities of several thousand can be achieved [46-49]. Hence, for planar spiral inductors it is clear that encapsulating the coils in magnetic material will enhance the inductance and allow for greater inductance values to be achieved with smaller device footprint.

2.2.2 Q-factor

The quality or Q-factor of an inductor characterises the efficiency of the inductor and is proportional to the ratio of energy stored to energy lost per cycle, hence:

$$Q = \frac{Energy\ stored\ per\ cycle}{Energy\ dissipated\ per\ cycle} \tag{2.8}$$

A perfect inductor will only consist of an inductive component. However, in reality inductors will be subject to losses in the coils and core. Hence, Q-factor can be described as being proportional to the ratio of inductance to effective resistance:

$$Q = 2\pi f \frac{L}{R} \tag{2.9}$$

The resistive component of the inductor is often modelled as a resistor in series with the inductor, and is termed as the equivalent series resistance. This value takes into account losses in both the coils and magnetic core [13, 50-54].

Typically, for inductors with magnetic cores, and at frequencies below the operational frequency, the Q-factor is greater than that of the equivalent air core inductor. From equation 2.9, this is intuitive as a result of the contribution to the inductance from the magnetic core. However, as frequency is increased past the operational frequency of the inductor with magnetic core, the inductance value decreases while the equivalent series resistance increases. Hence, the Q-factor of the inductor with the magnetic core will decrease below that of the air core inductor. The useful frequency of an inductor with magnetic core is the frequency at which the Q-factor of the inductor equals that of its equivalent air core inductor [13].

2.2.3 Loss Mechanisms

2.2.3.1 DC Resistive losses

DC resistive losses in the coil are the most basic loss mechanism. This loss in the coil is the result of resistive heating. The resistance of the coil is given by:

$$R_{coil} = \frac{\rho l_{coil}}{wd} \tag{2.10}$$

where ρ is the resistivity of the coil material, $w, d \; and \; l_{coil}$ are the width and thickness of the coil's cross-section, and the total length of the coil, respectively.

The material resistivity is sensitive to grain size, impurities, and inclusions [55, 56]. DC resistive losses for planar spiral inductors with $Ni_{45}Fe_{55}$ cores have been reported to be responsible for 23% to 73% of the total inductor losses [15, 28-31]

2.2.3.2 Eddy Currents

From Faraday's law, a voltage is induced in a conductor if it is subjected to a time varying magnetic field. Furthermore, as a result of Lenz's law a current will be produced by the induced voltage, which will generate a magnetic field to oppose the excitation magnetic field. Hence, when applied to power inductors, the magnetic field produced by the coil results in circulating currents forming in the conductive core. Subsequently these currents will form in such a way that they generate a magnetic

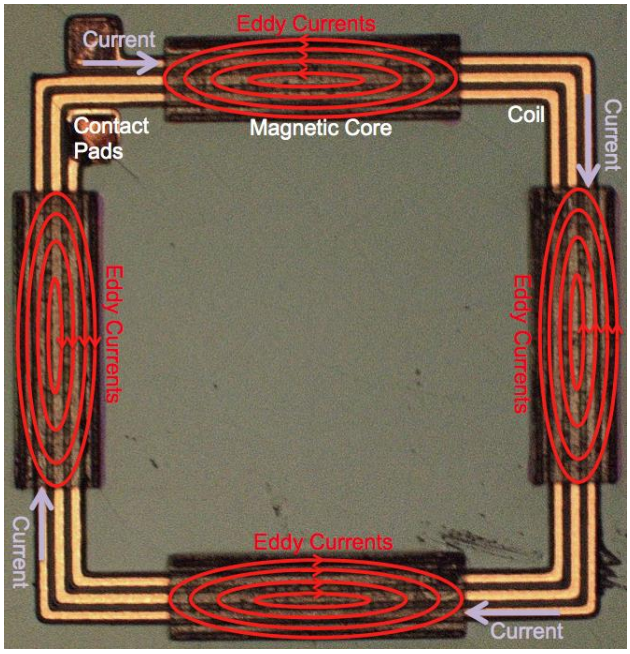


Figure 2.3: *Image of microinductors showing direction of excitation currents and eddy currents in the conductive magnetic core.*

field, which opposes the magnetic field produced by the coil. These currents are known as eddy currents. In addition to this loss mechanism eddy currents also induce resistive losses in the magnetic core [57]. An example of the formation of eddy currents in the magnetic core is presented in figure 2.3.

With sinusoidal excitation, eddy current power losses can be approximated by:

$$P_{eddy} = \frac{f^2 d^2 {B_{max}}^2}{6\rho} \tag{2.11}$$

Hence, the magnitude of eddy current losses is dependent upon frequency (f); core thickness (d); maximum magnetic flux density (B_{max}); and the electrical resistivity (ρ) [58-61]. This approximation typically calculates values of two to three times less than the measured losses resulting from eddy currents [61]. This difference has been widely reported on and is known as the eddy current anomaly [58, 61-67].

It is widely reported that power losses due to magnetic domain structure dynamics is the cause of this anomaly [58-60, 68, 69]. Bertotti [68, 69] has reported heating losses as a result of domain wall motion may be the mechanism responsible. These losses can be expressed as:

$$\frac{dW_A}{dt} = \left(\frac{GdbH_0}{\rho}\right)^{\frac{1}{2}}\left(\frac{dB}{dt}\right)^{\frac{3}{2}} \quad (2.12)$$

where W_A represents energy loss as heat, G is a dimensionless coefficient representing the eddy current dampening effect, d and b represent the width and thickness of the magnetic material, respectively. H_0 represents the statistical distribution of domain wall field and takes into account the material grain size [61, 68, 69].

Using finite element analysis (FEA) the eddy current losses in planar spiral inductors with $Ni_{45}Fe_{55}$ cores have been characterised to account for 10% to 43% of total losses [15, 28-31]. However, this analysis assumes the magnetic core consists of a continuous film. Therefore, eddy current losses may be significantly larger due to the eddy current anomaly.

2.2.3.3 Hysteresis Losses

A typical magnetic hysteresis loop is presented in figure 2.4. The area of the hysteresis curve represents the energy dissipated as heat during a single magnetization cycle [58]. Typically losses in the magnetic core resulting from magnetic hysteresis are determined by the empirical Steinmetz equation:

$$P_v = kf^{\alpha}\hat{B}^{\beta} \quad (2.13)$$

where $\hat{B}$ is the peak magnetic flux density, resulting from sinusoidal excitation. P_v is the average power loss per unit volume of magnetic material and f is frequency. The material parameters (k, α and β) are referred to as Steinmetz parameters, and are defined for limited flux density and frequency ranges [62, 70-72]. The hysteresis loop represents a number of physical properties, such as [73]:

Saturation magnetisation (H_S): The field applied which will not result in an increase in magnetic flux density. Hence, in this state all magnetic domains are orientated in the direction of the excitation field. The saturation magnetisation is an important property for power inductors, as this defines the inductor's saturation current [26].

Coercive field (H_c): The field required to restore the magnetic flux density (B) to zero.

Residual Magnetism (B_r): The flux density remaining, once the excitation field (H) has been removed.

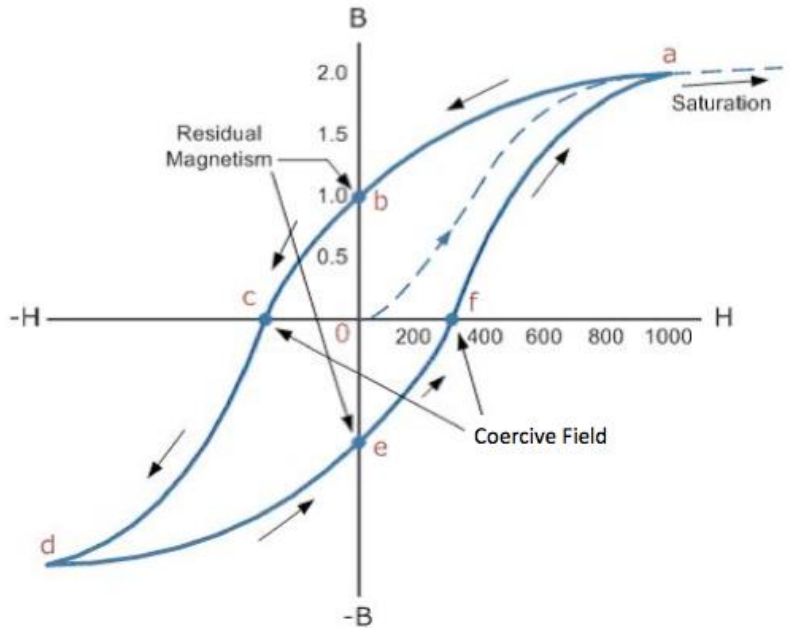


Figure 2.4: *Typical hysteresis loop [74].*

2.2.3.4 AC Resistive Losses

AC resistive losses are induced in the coil as a result of the proximity and skin effects.

A low frequency alternating current will flow throughout the conductor's entire cross-section. However, as frequency is increased, an increasing magnetic field at the centre of the conductor's cross-section will result in impedance to the current and the redistribution of current density to the edges of the conductor. This distribution of current density at the edge of the conductor is known as the skin effect and the depth into the conductor to which the current is constrained is known as the skin depth. A schematic of a conductor's cross-section, showing the skin effect is presented in figure 2.5. Skin depth (δ) is a function of frequency (f), the relative permeability (μ_r) and resistivity of the conductor, and is given by:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{2.14}$$

The net result of the skin effect is an effective decrease in the conductive cross-section, and hence increases in the conductor's resistance [75].

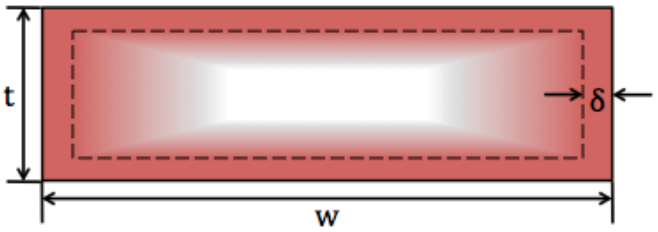


Figure 2.5: *Schematic cross-section of the permeability test structure showing the skin depth (δ).*

For materials, such as copper where the relative permeability (μ_r) equals 1, skin depth decreases with the square root of frequency, from equation 2.16. Hence the skin depth of copper decreases from 65µm to 21µm, as frequency is increased from 1MHz to 10MHz.

In addition to losses due to skin effect, AC resistive losses also occur due to the proximity effect. A conductor carrying a high frequency current can induce losses in the form of eddy currents in an adjacent conductor, this phenomenon is known as the proximity effect. Losses in the coil are induced as a result of increasing resistance. It should be noted that proximity effect is only pronounced at high frequency (greater than 100MHz) and hence many studies neglect this loss [42, 76, 77].

AC resistive losses have been consistently characterised to produce the lowest contribution to total losses (2% to 13%) for planar spiral inductors with $Ni_{45}Fe_{55}$ cores [15, 28-31].

2.2.3.5 Summary of Loss Mechanisms

Table 2.1 presents a summery of each loss mechanisms contribution to the total inductor losses reported in [15, 28-31]. It is clear from this table that the largest loss is a result of DC resistive losses, which arise from resistive losses in the copper coils. Hence, the most effective method to reduce device loss is to optimise the coil geometry.

Core losses consist of both eddy current and hysteresis losses and are influenced by core conductivity, volume fraction of magnetic material, thermal treatment and core geometry. One method of reducing these losses in the conductive magnetic core is to pattern the core. The influence of core patterning on inductance and Q-factor will be

investigated in chapter 5 and the effect on eddy current and hysteresis losses will be discussed.

AC resistive losses only occur at high frequency when the skin effect is pronounced. As inductors in this thesis will be measured up to 10MHz AC resistive losses will be negligible.

Loss Mechanism	%Loss
DC Resistive	23 to 73
Eddy Current	10 to 43
Hysteresis losses	10 to 29
AC Resistive Losses	2 to 13

Table 2.1: *Summary of loss mechanisms contribution to total inductor losses [15, 28-31].*

2.3 Fabrication Process

Microinductor fabrication processes involve a number of challenges such as the deposition of thick metal/dielectric layers; the patterning and gap filling of high aspect ratio trenches. Additionally, typical inductor fabrication processes have long lead times, which can result in challenges with the development and characterisation of new processes and materials with the inductor architecture.

An example of a planar spiral microinductor fabrication process is that developed by National Semiconductor in 2007. A top down view of a partially fabricated (bottom NiFe layer and copper coils only) inductor is presented in figure 2.6 (a), and a schematic cross-section of the completed inductor is presented in figure 2.6 (b). This inductor process has a number of characteristics similar to inductor processes presented in literature. For instance, electroplating is perhaps the most effective process for depositing metals layers of tens of microns thick. The use of electroplating has been employed in a number of spiral inductor fabrication processes reported in literature, specifically the electroplating of copper coils and NiFe has been reported in [9, 17, 77-87], and [85, 87], respectively. This architecture also incorporates an air-gap, which refers to a physical gap in the magnetic core filled with material whose relative permeability is one.

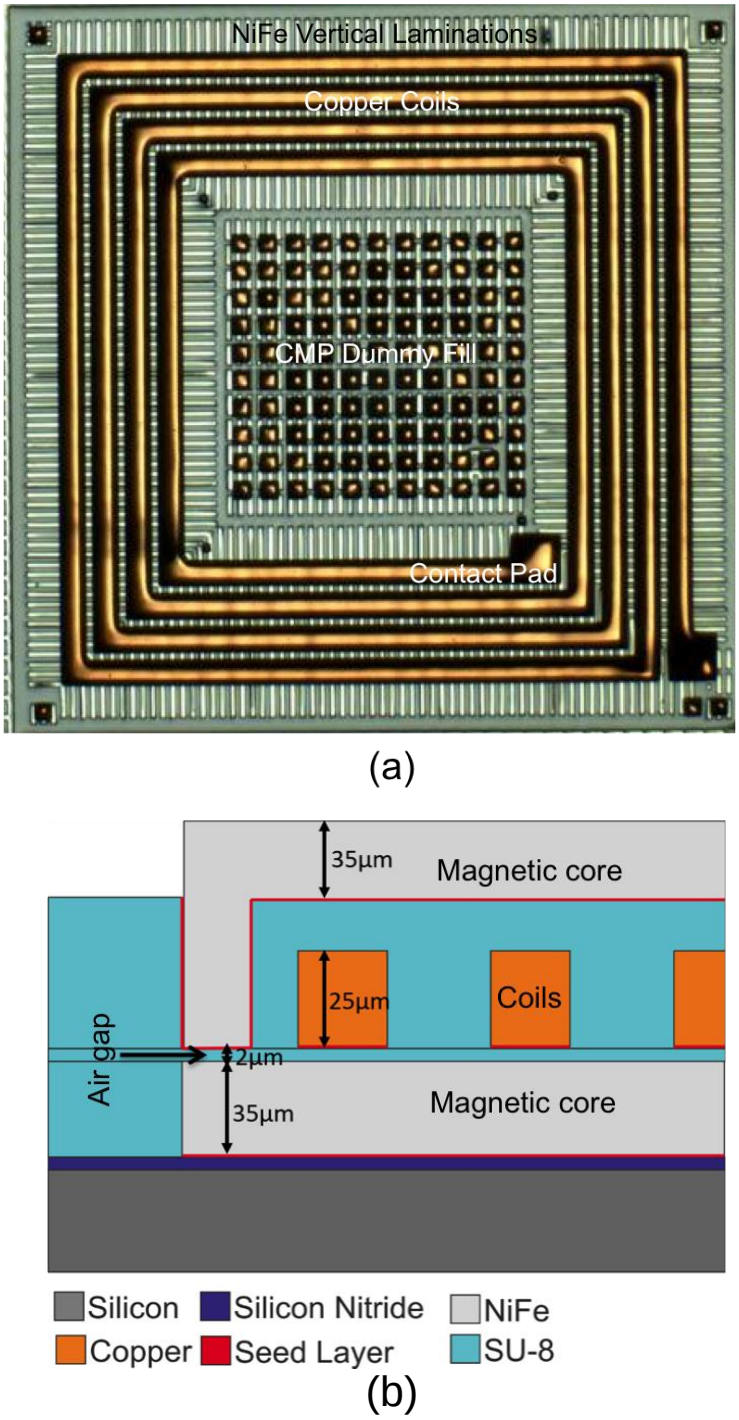


Figure 2.6: *(a) image of copper coils and bottom layer of NiFe, (b) schematic of cross-section through the copper coils.*

Additionally, the use of SU-8 as a dielectric and structural layer has been incorporated into many inductors [15, 18-31]. The complete National Semiconductor inductor fabrication process is presented in figure 2.7, and is described below:

(a) 1μm thick silicon nitride is deposited, which acts as an insulating and passivation layer for the silicon. Following this SU-8 is spin coated at 3400RPM and patterned to produce a film of 35μm thickness. This layer serves as a mould for electroplating of the bottom NiFe core and dielectric between vertical laminations.

(b) A seed layer is sputtered over the patterned topography (including the sidewalls). NR2-20000P is then spin coated at 2500RPM and patterned to produce a film of 28μm thickness. This layer is used to inhibit electroplating on top of the SU-8 and between the scribe channels.

(c) NiFe is conformally electroplated on to the SU-8 mould.

(d) The NR2-20000P is stripped; Ti-Cu- seed layer etched and the NiFe planarised to the top surface of the SU-8. Following this, 2μm of SU-8 is spin coated and patterned to act as an insulating layer between the bottom NiFe layer and copper coils. Additionally, this layer also forms an air-gap between the top and bottom NiFe layers.

(e) A Ti-Cu Seed layer is deposited. NR2-20000P is spin coated and patterned to act as a mould for the electroplating of the copper coils.

(f) Copper coils are electroplated to a thickness of 25μm. Following electroplating NR2-20000P is stripped and the seed layer is etched.

(g) 35μm thick SU-8 is spin coated and patterned to act as the inter-coil dielectric and structural layer. Additionally, this layer acts as a mould for the electroplating of the top NiFe layer.

(h) A Ti-Cu seed layer is deposited, followed by a NR2-20000P spin coating and patterning to inhibit plating on top of the SU-8 structure.

(i) NiFe is electroplated onto the SU-8 mould.

(j) NR2-20000P is stripped and seed layers etched. To complete the device over-plated NiFe is polished back and planarised with SU-8.

This fabrication process has a turn-around time of approximately one month, which is too long for it to be used as a test bed for the rapid development, integration and characterisation of materials and processes for microinductor fabrication. Hence it is

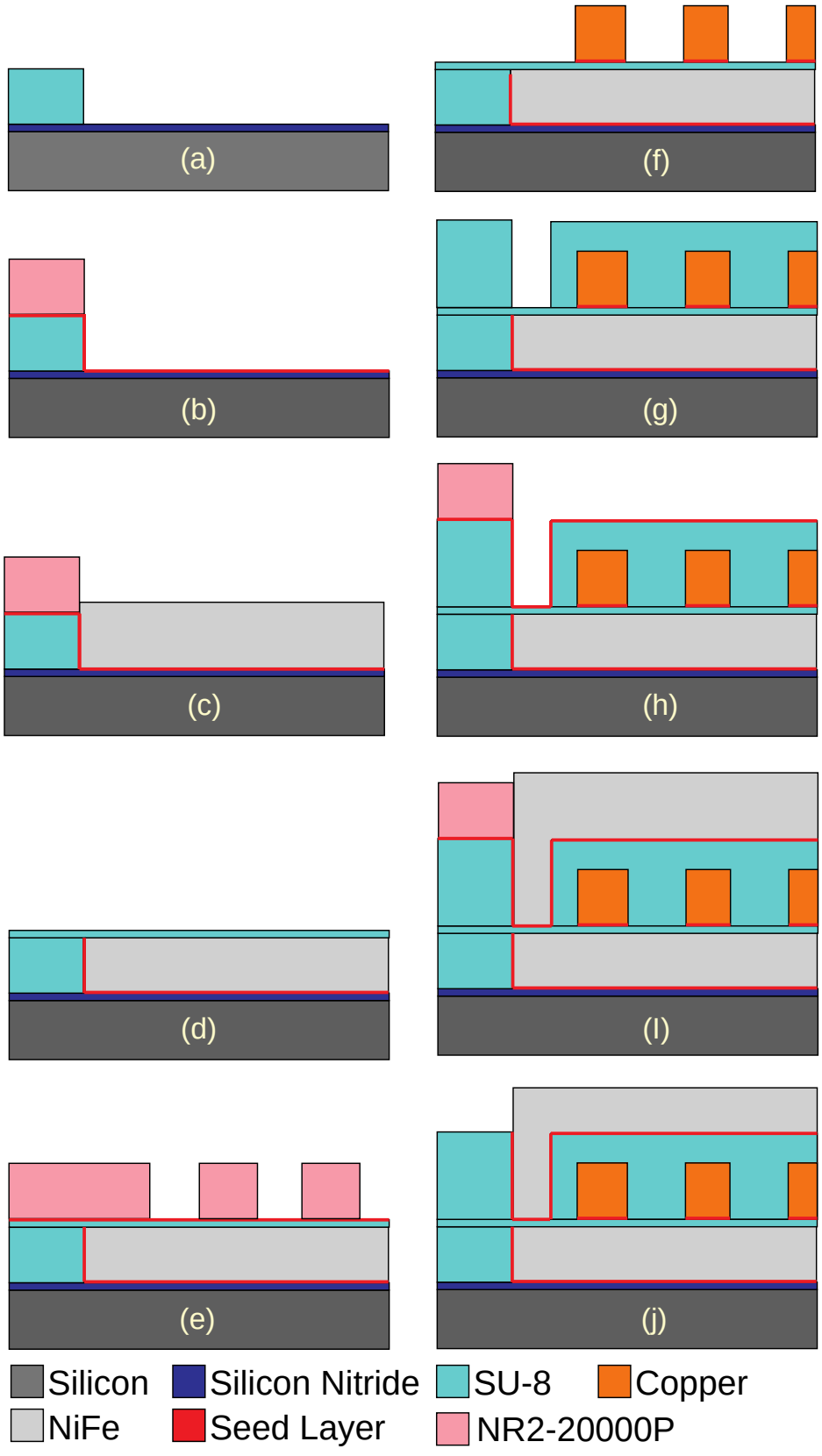


Figure 2.7: *National Semiconductor inductor fabrication process.*

desirable to develop a microinductor fabrication process with a much shorter turn-around time.

The following section reviews the materials and processes for use in the planar spiral microinductor fabrication process, by evaluating characterisation work reported in literature.

2.4 Electrochemical Deposition

Electroplating is an electrochemical process, which involves passing current through an electrolyte solution containing metal ions, which results in the deposition of metal onto an electrode's surface. For microinductor applications the use of electrochemical deposition for thick coils and core material is a common choice. Electrochemical deposition is an attractive choice for metal layer deposition due to its ability to deposit thick layers (tens of microns) in a single deposition. Additionally, bottom up plating though a resist mould would remove the need for dry etching or lift-off techniques that may be employed for the patterning of sputtered film. Typically, electroplating also has desirable qualities such as low cost, excellent pattern replication, gap filling properties and established and repeatable process. However, electrodeposited films often suffer from high residual stress, hydrogen embrittlement, self-annealing and inclusions from organic additives. These effects can impact upon the deposited films residual stress and conductivity. Additionally, the deposition process often requires the use of sputtered seed layers [41, 88-92, 94-97, 103].

2.4.1 Copper Electroplating

Electrodeposited copper is a typical choice for coil material due to its low electrical resistivity (1.68μΩ.cm) and low cost, simple, well-established, process. IBM first demonstrated the effectiveness of copper electroplating for IC technology in 1997. The proposed process detailed the damascene electroplating of copper and addressed the issue of depositing copper into vias and trenches without the formation of voids or seams [41].

For the work presented in this thesis, all copper electroplating has been carried out using the copper bath recipe detailed in table 2.2. The following chemical reactions described the electrodeposition of copper:

Copper	
Component	**Quantity**
Copper Sulphate	120.0 g/l
Sulphuric acid	190.0 g/l
Chloride	50 ppm
Additive - CVS	5.0 ml/l
Carrier - CVS	5.0 ml/l

Table 2.2: *Composition of the copper electroplating bath [88].*

The copper sulphate dissolves in water, as given by [88]:

$$CuSO_4(s) \longrightarrow Cu^{2+}(aq) + SO_4^{2-}(aq) \tag{2.15}$$

At the cathode either Cu^{2+} or water is reduced, as described by [88, 89]:

$$Cu^{2+}(aq) + 2e^- \longrightarrow Cu(s) + 0.32\,V \tag{2.16}$$

$$2H_3O^+(ag) + 2e^- \longrightarrow 2H_2O(l) + H_2(g) \tag{2.17}$$

Copper will more readily undergo reduction, and hence the final redox reactions are given by [88]:

$$2Cu^{2+}(aq) + 4e^- \longrightarrow 2Cu(s) \tag{2.18}$$

$$2H_2O \longrightarrow O_2 + 4H^+ + 4e^- \tag{2.19}$$

In addition to the electrolyte the electroplating bath also contain organics, denoted as additive and carrier in table 2.2. The additive and carrier act as accelerators and suppressors/brighteners, respectively. These organics are typically polyethylene glycol (PEG) and bis(sodiumsulfopropyl)disulphide (SPS). The combination of these two substances results in competition for the absorption sites which allows for void-free super-conformal damascene plating and the accelerated bottom up plating of submicron trenches [88-92].

The addition of the chloride ions in the plating bath has been noted to improve brightness in high current density areas of the film. The copper bath composition, detailed in table 2.2, introduces chloride ions (Cl^-) into the bath through the use of small volumes of hydrochloric acid. It should be noted that the inclusion of hydrochloric acid in an already very acidic bath would have no disadvantage. The small amount of chloride introduced into the bath is known to promote binding of the organic components to the cathode, which results in a more uniform plated film [88, 93].

The resistive properties of copper have been measured to decrease with time after electroplating. The sheet resistance of 1μm thick electroplated cooper has been measured to decrease from 6.1mΩ/□ to 0.951mΩ/□, whereas the sheet resistance of 20μm copper has been reported to decrease from 5.1mΩ/□ to 0.77 mΩ/□ over a 104-day period. This change in sheet resistance is the result of a phenomenon known as self-annealing, which results in the recrystallization of copper over time following electroplating. It has been reported that copper grain size relates to the sheet resistance of the film. Hence, this phenomenon results in increasing grain sizes and decreasing the sheet resistance, with time [94-97]. The effect of copper self-annealing has been studied by Huang [97] for a number of film thicknesses. The result of this study is presented in figure 2.8. This figure highlights three phases of copper self-annealing, For the first 500 min following electroplating the films exhibit an (I) incubation phase, regardless of film thickness. During this period a slight decrease in sheet resistance was measured. Following this films enter a transient phase (II) where there is a significant decrease in sheet resistance. The stagnation phase (III) occurs when sheet resistance reaches a steady state. Theses three phases and the shape of the curves reported in figure 2.8 are similar to those reported by Murray [98] and Yue [90]. However, Murray has determined that for the copper electroplating setup used in this thesis, the stagnation phase occurs 15 hours following electroplating for 3.5μm thick films plated using a current density of 20mA/cm^2 [98].

Whilst copper self-annealing will not be studied in this thesis, the reduction in sheet resistance in the hours following plating is beneficial for the reduction of resistive losses in the coil. Hence, sufficient time is left between electroplating and any measurements carried out on the copper coils, to ensure that self-annealing has reached stagnation phase and will not result in further changes to the electrical properties of the coil.

Inductors fabricated in this thesis use 30μm thick electroplated copper coils. While no studies have detailed this phenomenon for 30μm thick films, figure 2.8 shows that for

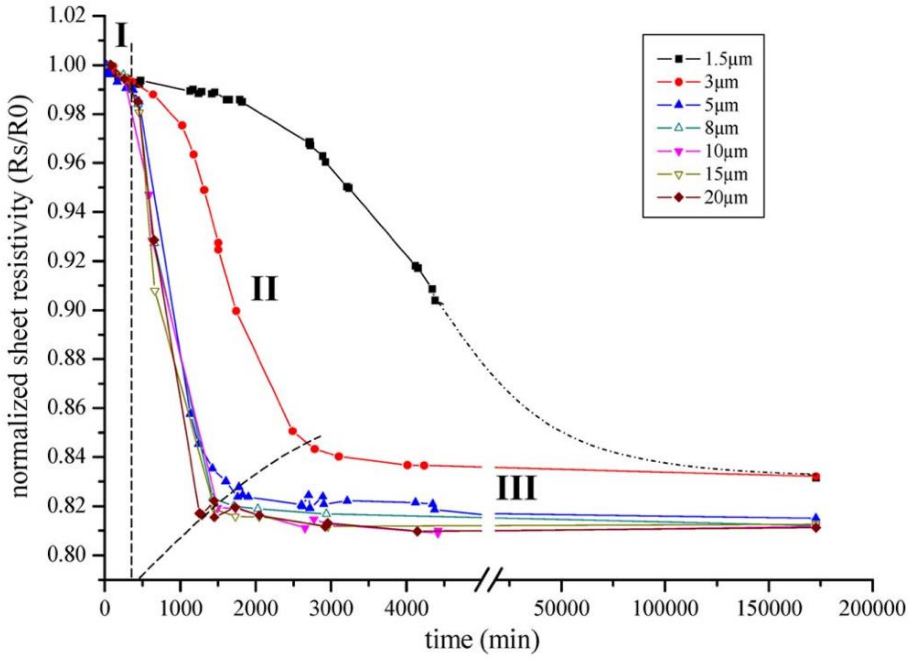


Figure 2.8: *Normalised sheet resistance, measured at discreet points following electroplating [94].*

thickness above 5µm the normalised sheet resistance converges to a constant value over time. Hence, it is postulated that 30µm thick films would also follow this trend.

2.4.2 NiFe Electroplating

Electroplated $Ni_{80}Fe_{20}$ (Permalloy) films are of particular interest for microinductor applications due to their high saturation flux density, relative permeability, low coercivity and magnetostriction [48, 99]. Arnold [100] has characterised the initial relative permeability of cast NiFe, which has been heat-treated at 900°C and allowed to gradually cool to 300°C. Following this, samples were annealed at 600°C before being allowed to cool to room temperature. In this study permeability was characterised for different NiFe alloys of the same size and geometry. Permeability measurements were taken at 5% Ni composition steps, except in the vicinity of $Ni_{80}Fe_{20}$ where a greater number of measurements were taken for a number of compositions. The initial relative permeability with respect to %Ni composition, measured using a ring permeameter, is presented in figure 2.9. It is clear from this figure that the optimum initial relative permeability is achieved with composition $Ni_{78.5}Fe_{21.5}$.

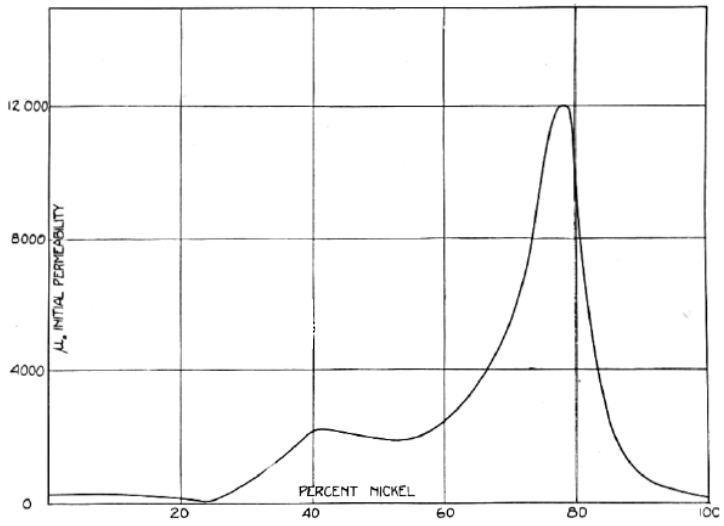


Figure 2.9: *Initial relative permeability of NiFe with respect to %Ni composition [100].*

The co-electrodeposition of NiFe to a precise ratio poses a significant challenge. As iron is a less noble metal, it will plate preferentially to nickel. To compensate for this the concentration of Ni^{2+} in the plating bath is significantly greater than Fe^{2+} [48, 101, 102]. The composition of the NiFe electroplating bath used in this thesis is presented in table 2.3.

Component	g/l
$NiCl_2$-$6H_2O$	109
$FeCl_2$-$4H_2O$	1.5
Boric Acid	25
Na Saccharin	2
Na Lauryl Sulfate	0.1

Table 2.3: *NiFe electroplating bath chemical composition [88].*

In addition to controlling the deposition rate, the current density also controls the NiFe composition [99, 101, 103, 104]. For the NiFe set-up used in this thesis the $FeCl_2$ content was optimised to produce electroplated films with $Ni_{80}Fe_{20}$ composition when plating with a current density of 10mA/cm^2.

As a result of the reduction of H^+ ions near the cathode to form hydrogen gas, the pH near the cathode increases gradually, which results in the formation of $Fe(OH)_2$, as given by [105]:

$$Fe^{2+} + 2OH^- \longrightarrow Fe(OH)_2 \qquad (2.20)$$

The $Fe(OH)_2$ absorb into the cathode much like the additive, where it is easily reduced to iron.

Hydrated nickel ions $(NiOH)^+$ inhibit reduction, and require higher energy to be reduced than iron. Nickel deposition can be described in two parts by the following [105]:

$$Ni^{2+} + H_2O \longrightarrow (NiOH)^+ + H^+ \quad (2.21)$$

$$(NiOH)^+ + H^+ + 2e \longrightarrow Ni + H_2O \quad (2.22)$$

2.4.2.1 Characterisation of Stress

Electrodeposited NiFe films suffer from high levels of residual stress, which will affect the reliability of the inductor device and can result in delamination of the NiFe layers. The residual stress level in NiFe films are reportedly influenced by processing parameters, such as concentration of electrolyte and saccharin. Additionally, annealing temperature and composition have been reported to effect residual stress. Figure 2.10 presents a comparison of NiFe stress levels reported in the literature.

The use of saccharin in NiFe electroplating baths has a number of advantages, having been reported by a number of studies to reduce residual film stress; promote small grain sizes and act as a leveller [103, 106-108]. Mishra [108] has reported that average grain sizes can be reduced from 24nm to 6nm, as saccharin concentration is increased from 0g/l to 6g/l. Subsequently, as saccharin concentration is increased the coercivity decreases from 1280A/m to 160A/m. Additionally, Lin [102] has reported that stress in the electrodeposited NiFe film decreases from 332MPa to 60MPa, as saccharin concentration is increased from 0g/l to 1.5g/l, for 2μm thick films plated at 6mA/cm^2.

Kagajawala [109] has reported the instantaneous stress in $Ni_{80}Fe_{20}$ during annealing at temperatures up to 170°C. Stress in the film has been reported to increase form 72MPa to 325MPa. It is noted that as the film is allowed to gradually cool to room temperature the stress in the film will decrease to 225MPa. Hence, thermal budget must be carefully considered when developing inductor fabrication processes containing NiFe layers.

Using the wafer bending method, the effect of electrolyte concentration on the residual stress of the electroplated NiFe film has been studied by Zhang [99]. This study

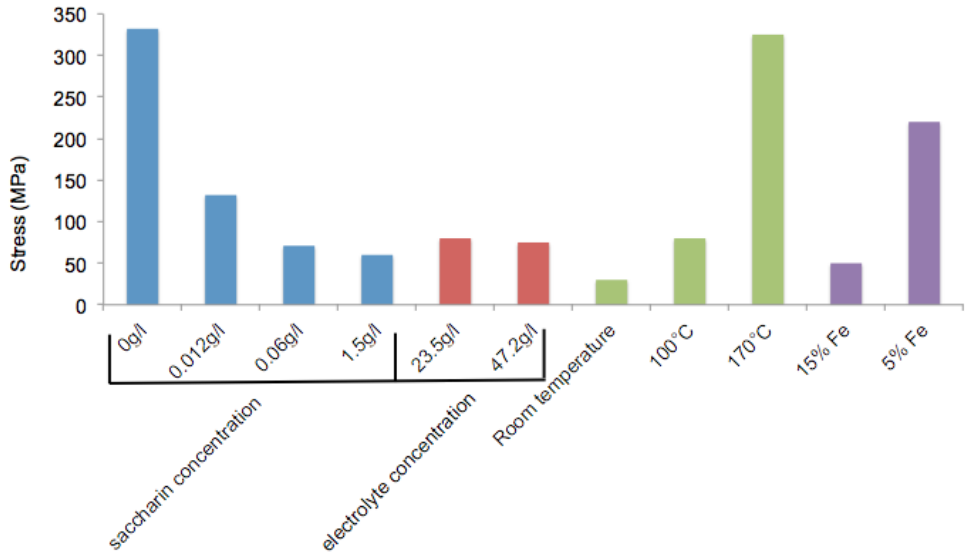


Figure 2.10: *Comparison of electroplated NiFe stress, reported in literature [37, 99, 102, 109].*

details the characterisation of the effect of two $NiCl_2$ electrolyte concentrations (23.5g/l and 47.2g/l) on the residual stress of the electroplated NiFe film. As is clear from figure 2.10, it has been determined that the electrolyte concentration has little effect on residual stress, where stress was measured to be 80MPa and 75MPa for 23.5g/l and 47.2g/l $NiCl_2$ concentration, respectively.

The spatial variation in stress has been characterised by Schiavone [37] for NiFe films where the composition across the wafer varied from 5% to 15% Fe. This study employed automated wafer mapping of strain indicator structures, and independent nanoindentation measurements to determine the spatial variation in Young's modulus. It has been reported that the residual stress is inversely proportional to the %Fe composition and is shown to increase from 50MPa to 150MPa, as the %Fe is decreased from 15% to 5%. The technique described in this paper will be employed in chapter 4 for the characterisation of stress in dielectric layers.

2.4.2.2 Characterisation of Permeability

As mentioned earlier in this chapter, the relative permeability of the magnetic core contributes directly towards the performance of the inductor. Hence it is desirable to achieve large values of permeability. A number of electroplating bath setup parameters contribute towards the achieved relative permeability of the electroplated NiFe film.

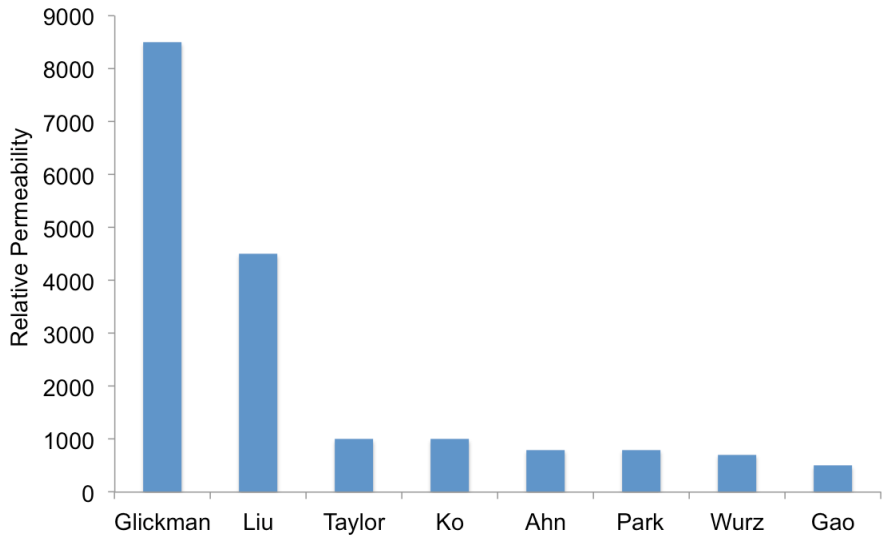


Figure 2.11: *Comparison of electroplated $Ni_{80}Fe_{20}$ initial relative permeability, at low frequencies reported in literature [11, 48, 106, 110-115].*

Figure 2.11 presents a comparison of achieved initial relative permeability reported in literature.

Glickman [48], achieved the highest permeability values reported through the use of an array of oscillating parallel fins to accomplish uniform agitation across the wafers surface, which allows for uniform diffusion of iron in the deposited film. It has been reported that non-uniformities lead to increased coercivity and decreased permeability. Additionally, the electroplating bath is maintained in an inert nitrogen environment, which prevents the reduction of Fe^{2+}, as given by:

$$2Fe^{2+} + 2H^{+} + {}^{1}/_{2}\,O_2 \longrightarrow 2Fe^{3+} + H_2O \qquad (2.23)$$

The Fe^{3+} can form an insoluble iron oxide, which results in contamination of the deposited thin film and hence a reduction in permeability.

Liu [110, 111] has achieved an initial relative permeability of 4500. However, the electroplating bath setup and testing method were not detailed. Other values presented in figure 2.11 report typical values of initial relative permeability from 500 to 1000.

The ability to perform permeability measurements on wafer has not been reported in the literature. This characterisation technique would provide an opportunity to provide fast feedback on the magnetic performance of Permalloy depositions, which is a capability, required for process control and verification measurements.

2.5 Dielectrics

2.5.1 SU-8

As with the National Semiconductor inductor fabrication process, SU-8 is commonly used as a dielectric and structural layer in MEMS inductor fabrication processes [15, 18-31]. SU-8 is an epoxy based negative photoresist, which was initially developed by IBM for use in high aspect ratio MEMS devices [116]. In inductor fabrication, SU-8 is attractive as it can be used as both a mould for electroplating, and structural layer in a single deposition. One of the most desirable properties of SU-8 is that it can be spin coated to a thickness of 2mm in a single deposition, where 40:1 aspect ratios have been achieved [32, 33]. At wavelengths above 400nm, SU-8 is transparent and wavelengths shorter than 350nm tend to be absorbed at the surface of the resist. Hence, wavelengths greater than 350nm can be used to achieve high penetration depths and thereby pattern thick layers [33, 117, 118]. The chemical structure of SU-8 is presented in figure 2.12. The eight reactive epoxy components enable a high degree of crosslinking following photo-activation [119]. Fully cross-linked SU-8 has a degradation temperature of approximately 380°C [117, 120]. This high degree of cross-linking contributes towards thermal and chemical stability [120-122]. Hence, the ability to pattern thick layers; with high thermal and chemical stability is desirable characteristic for a number of inductor applications. The SU-8 formulation has been improved upon in the MicroChem SU-8 2000 and SU-8 3000 products, which have distinct mechanical properties, with newer formulations designed to improve adhesion and reduce residual film stress [123].

2.5.2 Deposition Process

The SU-8 deposition processing parameters have been reported to affect adhesion and residual stress, which will subsequently affect the reliability and yield of the fabricated inductor. An outline of the SU-8 deposition process is presented in figure 2.13.

In order to improve adhesion the substrate is first cleaned, usually using piranha etch (3:1 sulphuric acid to hydrogen peroxide), or O_2 ashing. Following this, the wafer is dehydrated at 200°C. Next wafers are spin coated with SU-8, where spin speed and

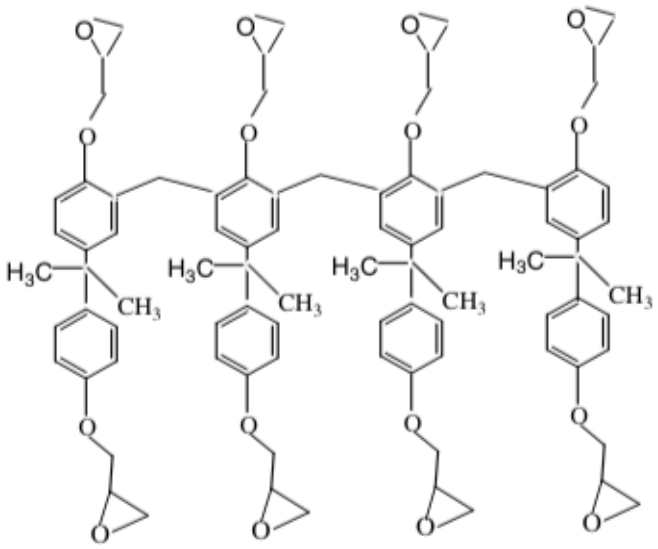


Figure 2.12: *Chemical structure of the SU-8 molecules [119, 120].*

time control the film thickness. A soft bake is used to evaporate the solvent from the film. Typically, this involves two baking steps, one at 65°C followed by one at 95°C. The exposure process is used to selectively activate the resist and release photo-acid, which is used to catalyse cross-linking. The post exposure bake process is used to cross-link the SU-8. Again, this is typically a two part baking process, with one step at 65°C followed by 95°C. Developing is used to remove uncross-linked SU-8 and define the pattern. Finally, the hard bake step is used to fully cure the resist and ensure no changes in the thermal properties during any following thermal processing [120].

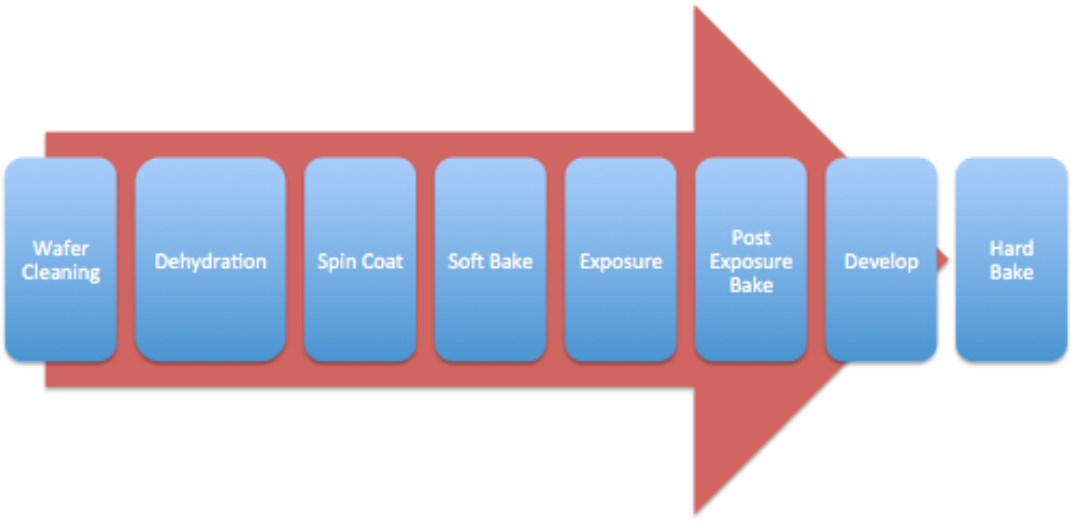


Figure 2.13: *Outline of SU-8 deposition process*

Table 2.4 presents the processing parameters recommended by Microchem compared to those optimised by National Semiconductor for the deposition of 50μm thick SU-8. The National Semiconductor process is similar to that outlined in the SU-8 datasheets. However, following soft and post exposure bakes at 95°C the wafer was further baked at 65°C. This step reduces the thermal shock from wafers being quenched at room temperature, and reduces residual stress in the film. Additionally, the exposure energy outlined in the National Semiconductor process is greater than those detailed in the datasheet as this has been optimized for the desired geometry.

2.5.3 Adhesion Characterisation

Delamination of SU-8 has been reported a number of times in literature [35, 124, 125]. Quantitative evaluation of SU-8 adhesion to a number of metals, silicon and silicon nitride has been detailed in [32, 126]. In both papers, SU-8 was spin coated and cured on top of the material under test. The testing setup is presented in figure 2.14, where (a) shows the tensile testing rig setup and (b) shows the sample setup [126]. Epoxy glue has been used to attach the sample to the grippers. The adhesion of SU-8 to Si, Ti, Au, and Al has been characterised in these papers. Dai [32] presents a similar adhesion testing setup. However, SU-8 was fabricated into circular test structures, and during tensile testing the wafer was held in place by a vacuum chuck, in accordance with standard ASTM-C633.

As the adhesion force is dependent upon the film's contact area, the adhesion of SU-8 will be characterised in term of adhesion strength (σ_a), which is defined as force measured at separation (F_{sep}) of SU-8 to material under test, per contact area (A), hence:

$$\sigma_a = \frac{F_{sep}}{A} \tag{2.24}$$

Figure 2.15 presents the adhesion force measured between SU-8 and each material under test, and compares this to the adhesion strength measured by SU-8 distributer MicroChem [127].

	MicroChem Datasheet Process			National Semiconductor
Deposition Step	**SU-8 50**	**SU-8 2050**	**SU-8 3035**	**SU-8 50**
Wafer Cleaning	Piranha Etch	Piranha Etch	Piranha Etch	O2 Ash, 400W
Dehydration	200°C, 5min	200°C, 5min	200°C, 5min	-
Spin Coating	1. 500rpm, 100 rpm/sec, 5 sec. 2. 5000rpm, 300rpm/sec, 30 sec	1. 500rpm, 100 rpm/sec, 5 sec. 2. 4000rpm, 300rpm/sec, 30 sec	1. 500rpm, 100 rpm/sec, 5 sec. 2. 3000rpm, 300rpm/sec, 30 sec	1. 3400RPM, 50RPM/sec, 70 sec 2. 5000RPM, 5000RPM/sec, 2 sec
Soft Bake	1. 65°C, 5min 2. 95°C, 15min	1. 65°C, 0-3min 2. 95°C, 6-9min	95°C, 10-15min	1. 65°C, 1min on pins, 5min contact 2. 95°C, 1min on pins, 15min contact 3. direct transfer from 95°C to 65°C
Exposure	175mJ/cm^2	150-250mJ/cm^2	150-250mJ/cm^2	246mJ/cm^2
Post Exposure Bake	1. 65°C, 1min 2. 95°C, 4min	1. 65°C, 1-2min 2. 95°C, 6-7min	1. 65°C, 1min 2. 95°C, 3-5min	1. 65°C, 1min pins, 1min contact 2. 95°C, 1 min pins, 5min contact 3. 65°C, 1min contact, 1min pins
Develop	ethyl lactate or diacetone alcohol 6 min develop time	ethyl lactate or diacetone alcohol 5-7min develop time	ethyl lactate or diacetone alcohol 6-12 min develop time	PGMEA spray develop, IPA rinse
Hard Bake(optional)	150-200°C	150-200°C, 5-30 min	150-200°C	150°C , 1min pins, 10 contact, 1min pins

Table 2.4: *Comparison of SU-8 deposition process recommended by Microchem compared to that optimised by National Semiconductor*

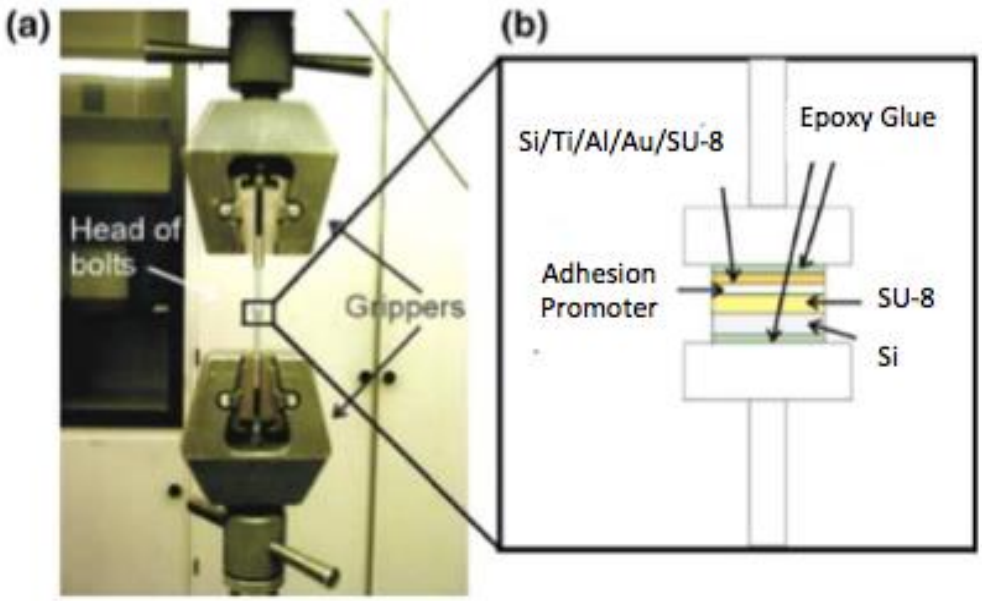


Figure 2.14: *Adhesion Testing setup, (a) presents the tensile testing setup, (b) presents sample configuration with adhesion of Au to SU-8 under test [126].*

The adhesion strength of 100μm thick SU-8 on Ti, Ni, Cu and Au (0.07MPa, 0.045MPa, 0.056MPa and 0.071MPa, respectively) reported by Dai [32], is reported to be lowest measured adhesion strength. This is likely the result of greater residual stress due to the elongated post-exposure baking time of 120 minutes.

MicroChem [127] consistently measure the highest adhesion strength with all materials tested. As SU-8 3000 is reported to include an adhesion promoter, it is not surprising that the adhesion strength of this formulation is consistently greater than that of the 2000 formulation. However, Microchem provide no details relating to the film thickness; exact processing conditions; or adhesion testing methodology used to obtain these measurements.

Hong [125] studied the effect of exposure energy, and post exposure bake temperature and time on the delamination of SU-8, on silicon substrates. It has been reported that the post exposure bake (PEB) is critical in determining if SU-8 will delaminate. It has been noted that for sufficient cross-linking a sufficient PEB time is required. However, above 70°C resulted in high degree of delamination. This has been attributed to the coefficient of thermal expansion mismatch between SU-8 and silicon. This paper does not detail the type of SU-8 used, or the effect of substrate preparation and hard baking

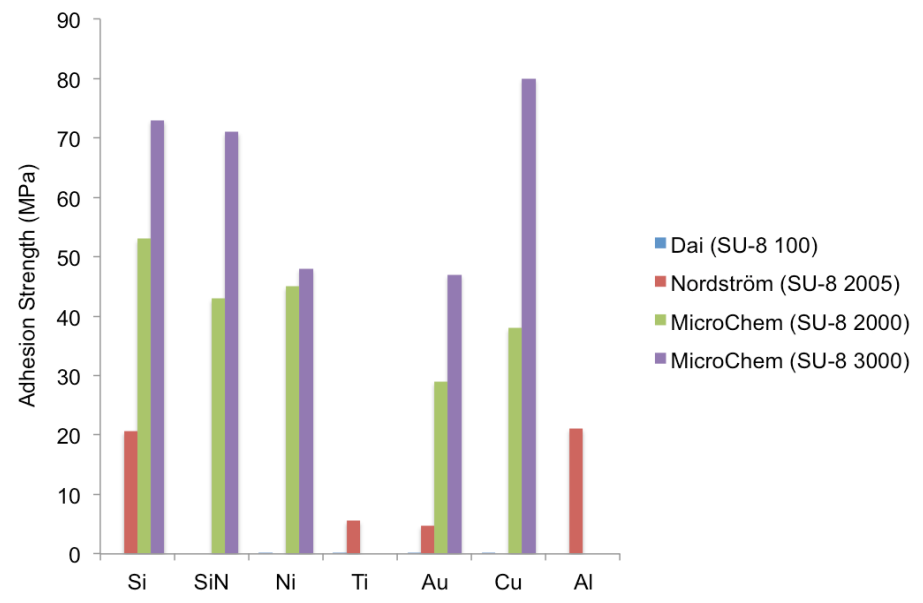


Figure 2.15: *Comparison of adhesion strengths reported in literature [32, 126-128].*

on adhesion. However, this result is surprising as all datasheets and all other literature indicates that a temperature of 95°C is required during post-exposure bake.

2.5.4 Characterisation of Residual Stress

As has already been mentioned, SU-8 suffers from intrinsic issues with high residual film stress, which can affect the reliability and yield of the fabricated inductor. However, the mechanical properties of SU-8 are strongly affected by processing conditions.

Residual stress in SU-8 films has been characterised by a number of papers [120, 129-131]. Typically, the residual stress in films deposited onto silicon wafers is determined by measuring the curvature of the wafer, and calculating the film stress (σ_f) using the Stoney formula [132-134]:

$$\sigma_f = \frac{E_s t_s^2 k}{6 t_f (1-v_s)} \tag{2.25}$$

where the subscripts f and s denote thin film and substrate, and E, v, t, k denote Young's modulus, Poisson's ratio, thickness and wafer curvature, respectively.

Lorenz [130] has used the wafer curvature method to characterise the residual stress in 20µm thick SU-8. This study has noted that the spin coating, soft bake and exposure steps have minimal contribution to residual stress in the film, and attributed the development of stress predominantly to the post-exposure and hard bakes. Wafer bow

was continually measured during thermal treatments and it was reported that the largest increases in wafer bow was measured during heating to the 95°C post exposure bake temperature (87.5%); heating to 200°C hard bake temperature (316.7%) and cooling following hard bake (76.9%). As was noted by Feng [120], the increase in wafer bow during post exposure and hard baking is likely the result of cross-linking occurring during these thermal treatments. The increase in wafer bow during cooling from the hard bake temperature is likely the result of shrinkage of the SU-8 film and coefficient of thermal expansion mismatch. The maximum stress in the film was measured to be 17.4MPa, for 400μm thick SU-8, which has not undergone hard baking.

Wouters [135] employed the use of strain indicator structures, as presented in figure 2.16, to characterise the residual stress in SU-8 2050. Stress was reported to be 18MPa. Young's modulus was determined to be 2.1GPa, using tensile testing. Samples were prepared on Teflon films, and following the developing stage, peeled from the Teflon film. Samples were post exposure baked at 95°C, once again without any hard bake.

The SU-8 hard baking process will improve the thermal and chemical stability of the SU-8 film, and is required for inductor fabrication processes where SU-8 remains part of the structure. Hence, it is important to characterise the residual stress as a result of hard baking

While Wouters [135] has employed the use of the strain indicator structure presented in figure 2.16, many other strain indicator structures using expanding/contracting beams connected to a rotating pointer arm to indicate strain in the plane of the layer,

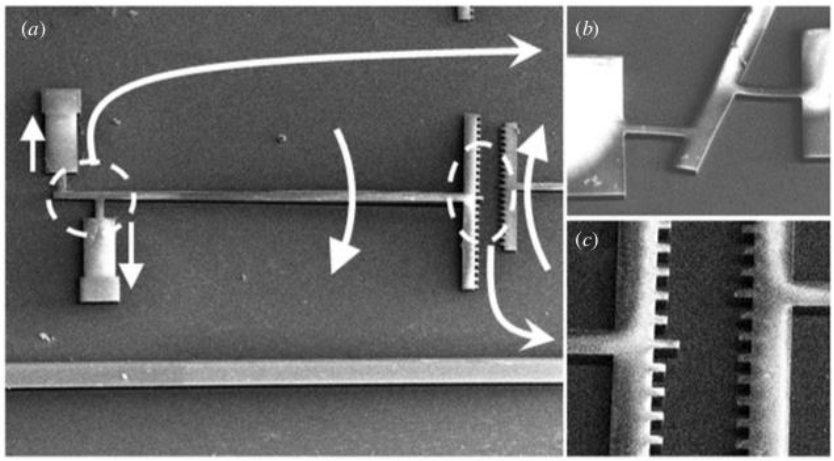


Figure 2.16: *(a) Strain indicator structure, indicating tensile strain, (b) close ups of flexible hinges and (c) vernier grating [135].*

have been reported in literature [37, 98, 136-139]. Many other test structures for the measurement of strain in the film have also been published, including the buckling bridge [138, 140, 141]; Guckel ring [138, 142]; load deflection membrane [143, 144] and cantilever test structures [37, 139, 145-147].

Strain indicator structures will be used in this thesis for the characterisation of strain in dielectric and NiFe layers. The strain test structures used in this work have been reported in [37, 98, 136, 137]. These structures were selected as a result of their simple fabrication process, and the already available and well-defined measurement setup and methodology.

2.6 Benchmarking

To determine the current state of the art, it is necessary to benchmark inductors reported in literature. A comparison of inductance value (at 10MHz) against number of turns is presented in figure 2.17. This figure clearly highlights increasing inductance with number of turns, and hence the requirement to increase the number of turns to achieve higher inductance values.

Figure 2.18 presents a comparison of Q-factor against inductance density; this comparison has been reported by Gardner [148]. With the current trend toward further reduction in component sizes, the performance per unit area (inductance density) is critical. Additionally, plotting Q-factor against inductance density will present the relationship between inductor efficiency and performance. Clearly, it would be desirable to produce inductors with inductance and Q-factor values such in the top right corner of this graph. However, typically altering inductors architecture to improve performance also increases losses, and subsequently reduces Q-factor.

From the data presented it is observed that the largest Q-factor (22) has been achieved by Bae [84] with a 2.5 turn inductor, with $Ni_{50}Zn_{30}Cu_{20}$ ferrite core. The resistivity of NiZnCu ferrite films, deposited using a two-step sintering process, has been reported to be in order 10^{10} Ω.cm [149]. Hence, this high Q-factor is likely the result of insignificant core electrical losses. The drawback of using the architecture reported in [84] is that the magnetic core deposition process requires the sputtering of five films followed by heat treatment at 800ºC. To achieve a high Q-factor, the inductor reported by Bae [84] clearly highlights the need to mitigate eddy current losses in the magnetic core.

Figure 2.17: *Comparison of inductors reported in literature, where inductance (at 10MHz) is plotted against number of turns [9, 77-87].*

From figure 2.17, Wang [86] reported on 3 turn inductors with $Ni_{80}Fe_{20}$ cores including Cr laminations. These inductors achieve an inductance of 0.9nH, and an air core inductance of 0.33nH. Hence the inductance enhancement as a result of the inclusion of the magnetic core is 172%. The low inductance measured in Wang's work is the result of a small device footprint of 0.0016mm^2. However, this inductor produces the largest inductance density of 562.5nH/mm^2 reported in literature.

Zheng [87] reported 8 turn $Ni_{80}Fe_{20}$ core inductors, with inductance values of 170nH to 190nH and inductance densities from 4.17nH/mm^2 to 4.95nH/mm^2. These low inductance densities are the result of the architecture only having NiFe below and in the centre of the inductor coils. Clearly, encapsulating the coils with magnetic material will result in a greater improvement in inductance, and allow for smaller device footprints as the centre of the inductor can be utilised.

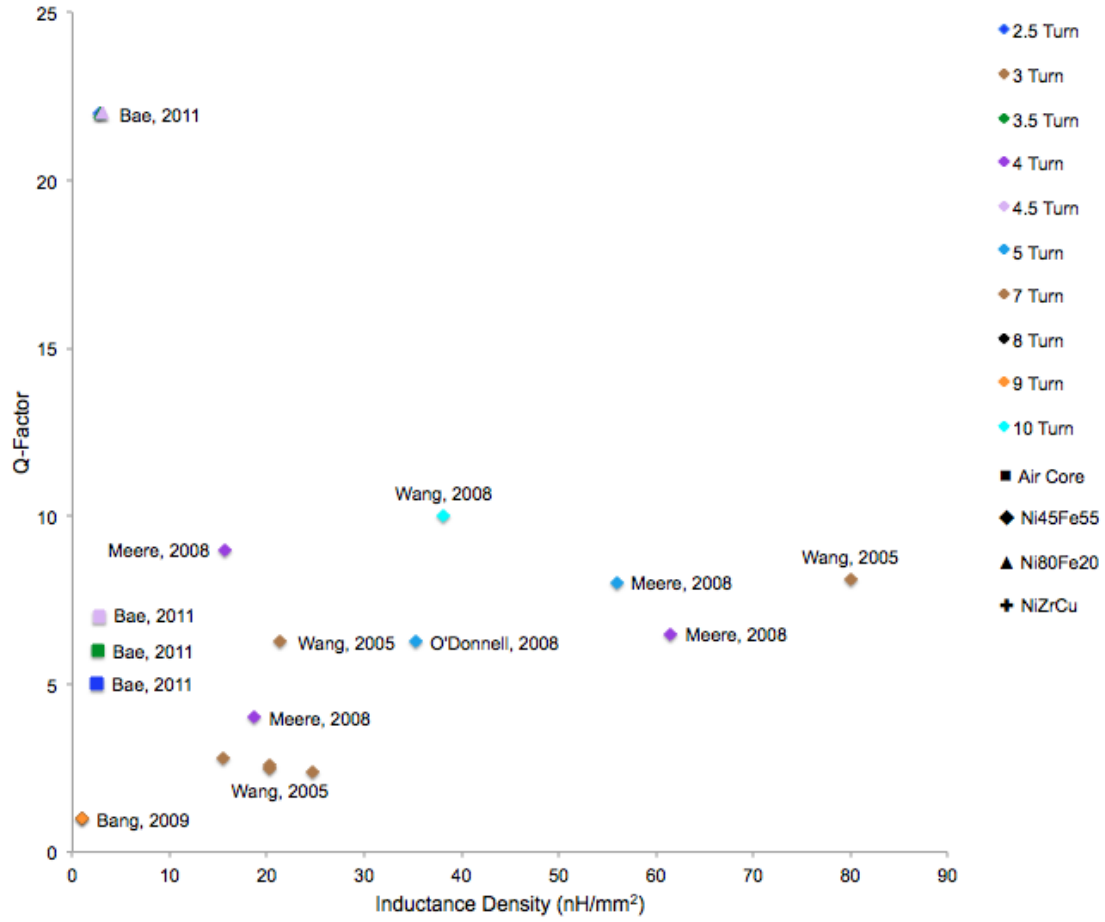


Figure 2.18: *Comparison of inductors reported in literature, comparing Q-factor to inductance density (at 10MHz) [9, 17, 77-87].*

2.7 Summary

This chapter has defined the parameters used to characterise the performance, efficiency, and loss mechanism of an inductor.

A microinductor process developed by National Semiconductor has been presented. This inductor fabrication process has a turn-around time of one month. Hence, for the characterisation of new materials and processes with the microinductor architecture it is desirable to develop a test-bed fabrication process with a much shorter turn-around time. The National Semiconductor inductor architecture includes many attributes typical of inductor architectures reported in literature, for example, the use of SU-8 as a dielectric and structural layer; electrodeposition of copper and NiFe as coils and magnetic core.

Literature which reports upon achieved permeability and residual stress has been

evaluated. However, it is noted that properties of the electroplated NiFe film such as permeability, electrical resistivity, and mechanical stress directly contribute to inductance value, eddy current losses and reliability of the fabricated device, respectively. However, no study has presented a characterisation of all of these properties. Furthermore, a method of characterising relative permeability on wafer has not been detailed in the literature. The ability to perform this measurement on wafer provides an opportunity to provide fast feedback on the magnetic performance of Permalloy depositions, which is a capability, required for process control and verification measurements.

Attention has also been draw to intrinsic problems with stress and adhesion in SU-8 films. From this review it is clear that there is a need to identify new materials for use as a structural and dielectric layer in microinductor processes.

Chapter 3
Characterisation and Integration of Parylene-C as a Structural and Dielectric Layer

3.1 Introduction

High aspect ratio metal structures are important for the development of high Q-factor integrated passive devices, such as microinductors. One of the most common methods used to fabricate micro-scale copper coils is to use SU-8 as a mould to define a trench, which is then filled with electroplated copper. One attraction of this approach is that the SU-8 becomes part of the structure providing the inter-coil insulator [31, 150, 151], thereby removing the requirement for any further deposition and lithographic steps associated with the inter-coil dielectric. However, as discussed in chapter 2, there are intrinsic problems with SU-8 associated with adhesion and mechanical stress [137]. The delamination of SU-8 has been reported in the literature [125, 152, 153] and has been observed in this work when SU-8 is processed on top of silicon, copper (sputtered), titanium (sputtered), and NiFe (electroplated). Hence, there is clearly an interest in identifying and characterising new processes and materials, both for filling of high aspect ratio gaps between metal coils and features, as well as minimising any mechanical stress resulting from the required thick layers. This is particularly the case when integrating thick copper coils with thick NiFe films.

One possible candidate to resolve these issues is the polymer, Parylene. This material is widely used as a protective coating on printed circuit boards (PCB) [34], as it can be conformally deposited from a vapour phase at room temperature. The properties of Parylene as an interlayer dielectric, along with its barrier properties, and inherent low stress deposition [153], make it an attractive candidate to replace thick SU-8 films as the insulator between the electroplated copper coils in microinductors. As Parylene is not appropriate for use as an electroplating mould, the architectures proposed in this work will use photoresist moulds that can be removed after electroplating. Once the photoresist is removed, the Parylene is then conformally deposited to insulate adjacent coils.

This chapter reports the development of test structures and processes to characterise the suitability of Parylene for integration into a planar inductor fabrication process. This involves the use of test structures consisting of trenches and tracks to assess the gap filling and insulation properties of vapour deposited Parylene. Adhesion tests have been performed to augment previously reported work [154]. The results of this characterisation are used to fabricate a complete microinductor, incorporating NiFe layers and Parylene.

3.2 Parylene Deposition Process

Parylene is deposited using a vapour deposition process, at room temperature. Szwarc [155] first observed the deposition of Parylene-n in 1947, through the vacuum pyrolysis of solvent para-xylene. The method used in this study was first realised by Gorham and involves the vacuum pyrolysis of dichloro-di-para-xylylene dimer [156, 157], which is outlined in figure 3.1. In this process, the dicholoro-di-para-xylylene dimer is heated to 150°C at 1 Torr in a vaporiser furnace. This results in the dimer sublimating into a dimeric gas. Following this, the gas is pyrolised to form the monomer chloro-para-xylene, which then polymerises on all surfaces inside the room temperature deposition chamber [157]. The thickness deposited is controlled by preloading the vaporiser furnace with a calibrated dimer mass. It has been reported that this will produce a film of thickness with error ±10% of the desired thickness [158].

An example of Parylene used in a MEMS inductor fabrication process is reported in [160] where Parylene-coated 2-D coils were folded on top of each other to produce a 14.6-mm-diameter 96-turn three-layer copper 3-D coil.

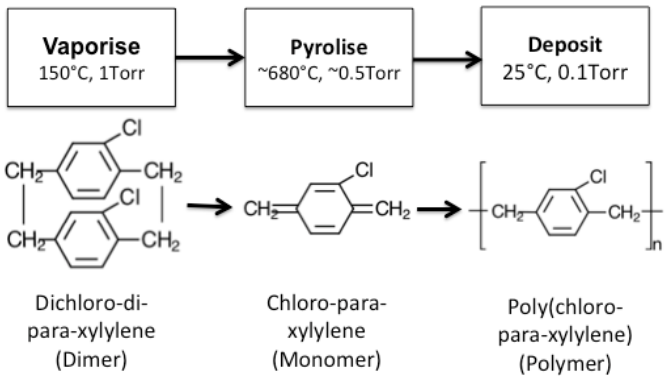


Figure 3.1: *Parylene-C deposition and polymerisation process [159].*

3.3 Microinductor Fabrication Process

As discussed in chapter 2, the patterned core inductor process, developed by National Semiconductor has a turn-around time of one month. To reduce the time required evaluating the suitability of materials and processes for fabricating magnetic components there was a need to develop a vehicle to rapidly test new materials and processes. This was achieved by developing a short turnaround test-bed inductor process. The reduced processing steps associated with using Parylene as a structural and dielectric layer proves to be an attractive proposition. Figure 3.2 presents the developed test bed inductor process flow.

The process description is detailed below:

(a) 1µm of silicon dioxide is first thermally grown to create an insulating layer between the substrate and bottom NiFe layer. Ti(30nm)-Cu(300 nm)-Ti(30nm) seed layers is then deposited using magnetron sputtering. Next, 5µm of NR2-20000P is spin coated and patterned, to act as a mould for electroplating NiFe.

(b) The top Ti layer is removed and the bottom layer of NiFe is electroplated using the NR2-20000P mould.

(c) NR2-20000P is then stripped, and the seed layer etched using a Cu etch solution then 1% HF for Ti. Next, 5 µm of Parylene is then deposited.

(d) Parylene is then planarised with the top surface of the NiFe layer. A further 5µm of Parylene is deposited to act as an insulating layer between the bottom NiFe layer and the coils.

(e) A Ti(30nm)-Cu(300nm)-Ti(30nm) seed layer is then deposited. NR2-20000P is then spin coated and patterned, to act as a mould for electroplating the copper coils.

(f) The copper coils are then electroplated. NR2-20000P was stripped, and the seed layer etched using 1% HF and a Cu etch solution, for Ti and Cu layers respectively.

(g) Next, 5 µm of Parylene is deposited over the electroplated coils.

(h) 35µm of NR2-20000P is then spin coated and patterned to act as an etch mask for Parylene etching.

(i) Using an O_2 reactive ion etch (RIE), Parylene is etched to a depth of 7 µm to create the magnetic vias, and expose contact pads.

(j) Following this, the NR2-20000P is stripped, and Parylene is planarised to the top surface of the copper coils using chemical mechanical polishing (CMP).

(k) A further 5µm of Parylene is deposited to act as an insulating layer between the coils and the top NiFe layer.

(l) Again, 35µm of NR2-20000P is coated and patterned to act as an etch mask for Parylene.

(m) Parylene is once more etched to a depth of 7µm to complete the magnetic vias and expose the contact pads. NR2-20000P is then stripped and Ti(30nm)-Cu(300nm)-Ti(30nm) magnetron sputtered.

(n) Following this, 35µm of NR2-20000P is then coated and patterned to act as a mould for electroplating the top layer of NiFe.

(o) 5µm thick NiFe is then bottom up electroplated onto the NR2-20000P to create the top NiFe core. This is followed by NR2-20000P strip and the seed layer is etched using 1% HF and Cu etching solution, to complete the inductor.

3.4 Characterisation of Parylene

In the fabrication process proposed in section 3.3 there were three main challenges: confirming good Parylene adhesion to films used in this fabrication process; ensuring Parylene fully and conformally fills gaps between high aspect ratio copper coils (step (g)); and developing a chemical mechanical polishing (CMP) process for the planarisation of Parylene over thick copper coils (step (j)).

3.4.1 Adhesion Testing

The first step was to evaluate the adhesion of Parylene to materials commonly used in inductor fabrication processes. Using the deposition process described in section 3.2, Parylene was deposited onto three-inch wafers coated with a number of patterned and substrate with a silane primer, which has been reported to improve Parylene adhesion to inorganics such as silicon and metals [143, 161, 162].

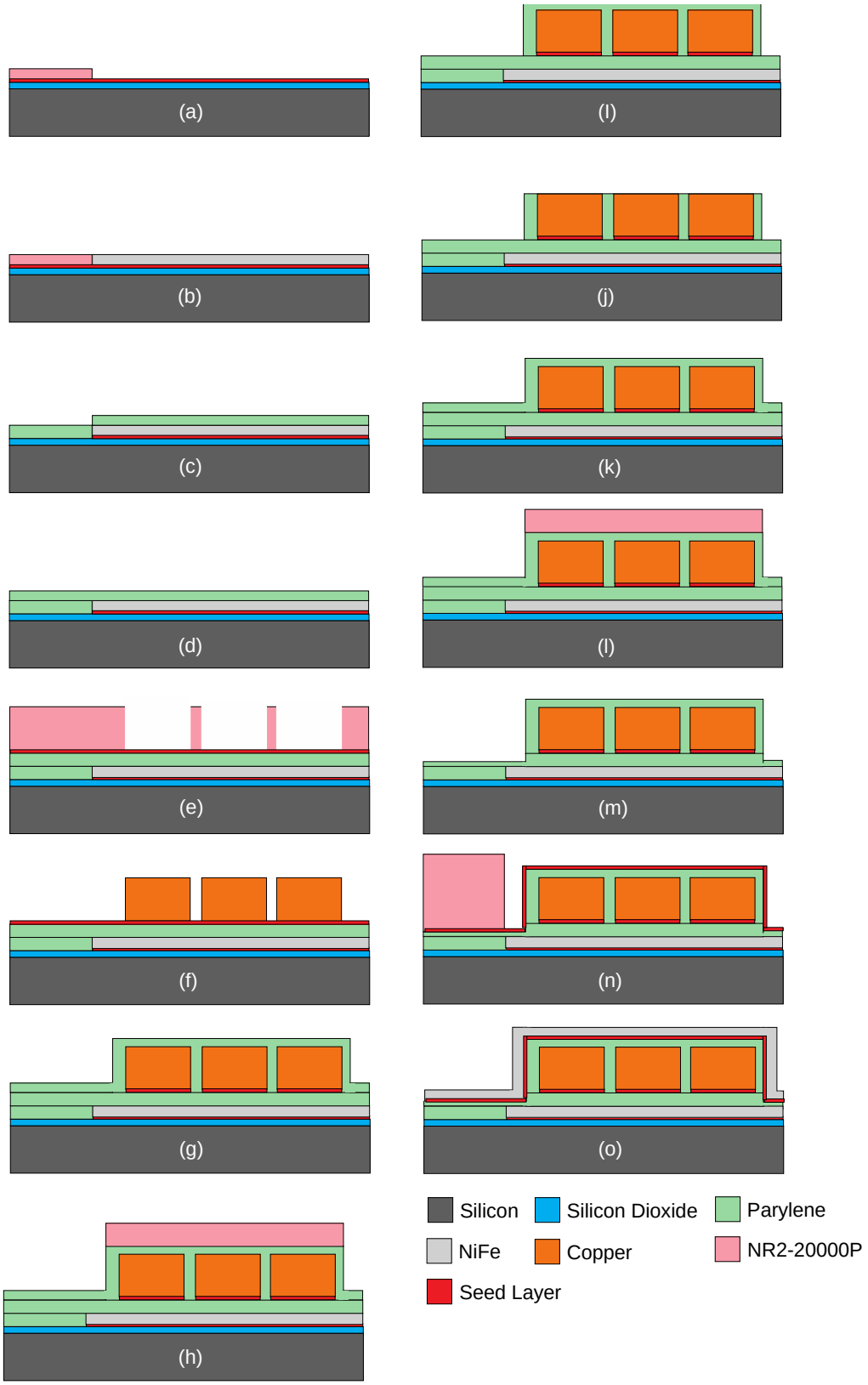


Figure 3.2: *Test bed planar spiral microinductor fabrication process.*

The method used to test the adhesion of Parylene to different layers is the "Scotch-tape" test [163, 164]. This is a qualitative adhesion testing method, first attributed to Strong [164] for the adhesion testing of evaporated aluminium films on glass substrates. This method involves pressing an adhesive tape against the layer under test and then rapidly stripping the tape off. As a result there are three possible outcomes: the film is completely removed from the substrate; the film is partially removed from the substrate; and the film is not removed from the substrate. Hence this testing method can only be used to screen cases of films with poor adhesion against those with acceptable adhesion.

Table 3.1 presents the films tested and the result of the Scotch-tape test, where a tick indicates that the film has presented no removal from the substrate. A dash indicates that this test has not been carried out. Therefore these results indicate that good adhesion can be achieved between all layers tested.

3.4.2 Test Chip for Parylene Fill Efficiency and Chemical Mechanical Polishing.

The fill performance between high aspect ratio copper structures is of interest as gaps formed during the conformal deposition of Parylene between copper coils (fabrication step (g)) may result in reliability issues. A test chip has been designed to evaluate the fill performance of Parylene, between thick copper tracks (30µm) with a range of aspect ratios (width:height), from 5:3 to 1:15. The fill performance between 1:3 aspect ratio structures will be of particular interest as this is the pitch of the inductor coil, which is to be fabricated.

The test chip consists of arrays of stripes/tracks with a range of widths (from 50µm to 10 µm) and separations (from 50µm to 2 µm); the layout is presented in Figure 3.3. The test chip also includes lithography test structures, resolution bars and checkerboards structures, to confirm the dimensions of the features for sectioning. Schematic drawings of these test structures are presented in figure 3.4. By optically unpatterned layers used in the proposed microinductor process flow. The standard process, prior to deposition is to coat the deposition chamber and ensuring that the edges of the checkerboards and resolution bars align it is possible to confirm that the features have been resolved at the desired feature size.

Material	Patterned	Unpatterned	Successful Completion of Scotch Tape Test
Silicon	-	✓	✓
Silicon Dioxide (Thermal Oxide)	-	✓	✓
Silicon Nitride (PECVD)	✓	✓	✓
Parylene-C	✓	✓	✓
Copper (Sputtered)	✓	✓	✓
Copper (Electroplated)	✓	✓	✓
Titanium (Sputtered)	✓	✓	✓
NiFe (Electroplated)	✓	✓	✓
SU-8 3005	✓	✓	✓

Table 3.1: *Scotch tape results to evaluate the adhesion of Parylene to a number of different materials commonly used in MEMS. A tick reports a pass, without any film removal. A dash reports that the test was not carried out.*

Chemical mechanical polishing (CMP) is used to planarise the Parylene with the top of the copper coils (fabrication step (i)). This ensures that the top NiFe core is electroplated on a planar surface and the magnetic core is a consistent distance from the copper coil. To ensure that the top surface of the coils is sufficiently planar, the test chip will be used to evaluate Parylene dishing between copper tracks, following CMP. In addition it will be necessary to evaluate surface roughness of Parylene after CMP to ensure that accumulative surface roughness, after depositing subsequent layers, will not be an issue.

The test chip was fabricated using a subset of the fabrication process described in section 3.2. Figure 3.5 presents the process flow, and a description of these steps follows:

(a) 1µm of silicon dioxide was first thermally grown onto the silicon substrate. Following this a Ti(30nm)-Cu(300nm)-Ti(30nm) seed layer is deposited.

(b) NR2-20000P is spin coated and patterned to act as mould for the bottom up electroplating of the thick copper tracks.

(c) Copper tracks are electroplated, after which the photoresist is removed.

(d) Parylene is then deposited. It is at this point that half of the batch will be sectioned to evaluate Parylene fill between the high aspect ratio copper tracks.

(e) The other half of the batch will undergo CMP to evaluate Parylene dishing between copper tracks and surface roughness of Parylene following CMP.

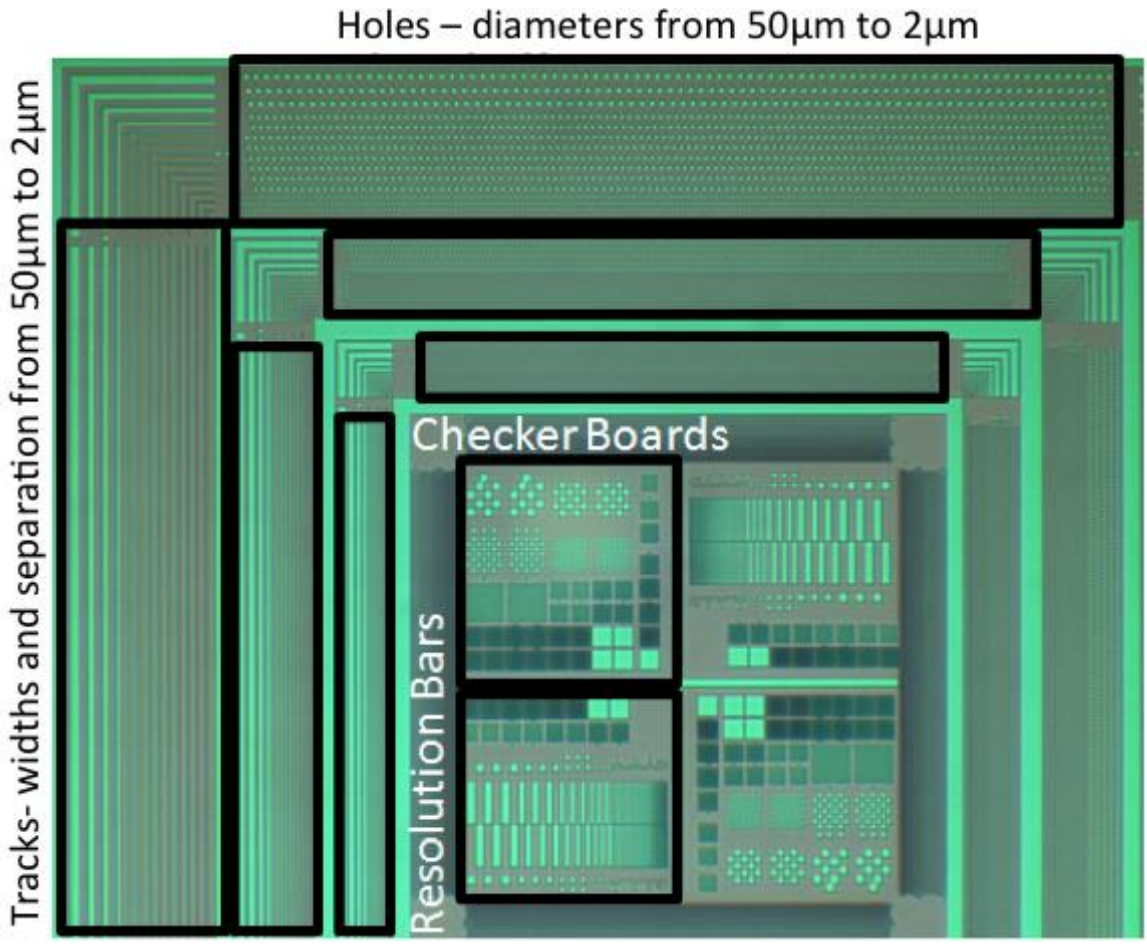


Figure 3.3: *Layout of the test chip (10×10mm) with arrays of tracks with various widths and separation between tracks.*

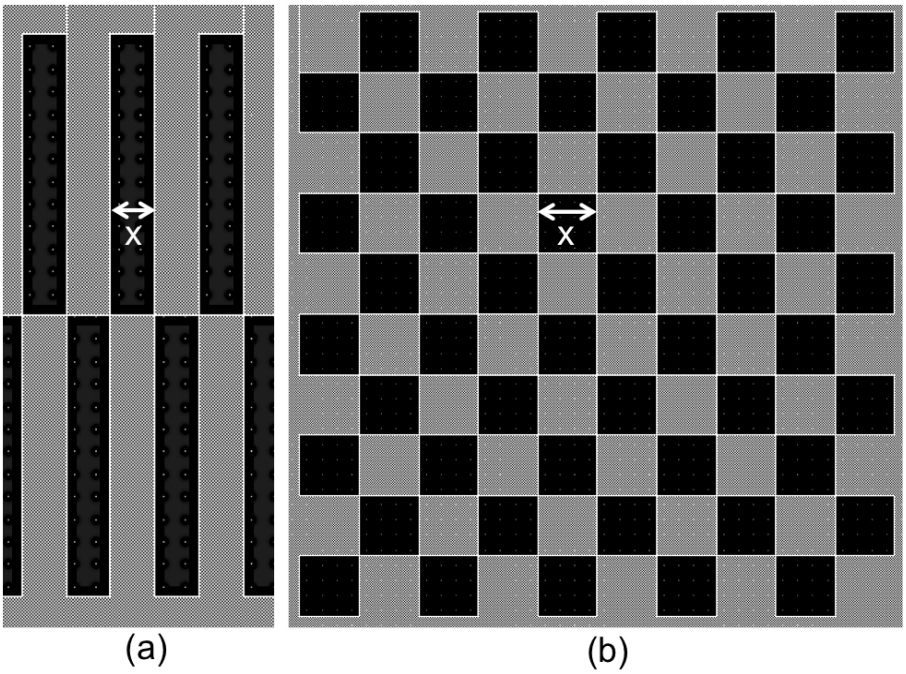


Figure 3.4: *Lithography test structures, (a) resolution bars and (b) checkerboards. the value of x varies from 50µm to 2µm.*

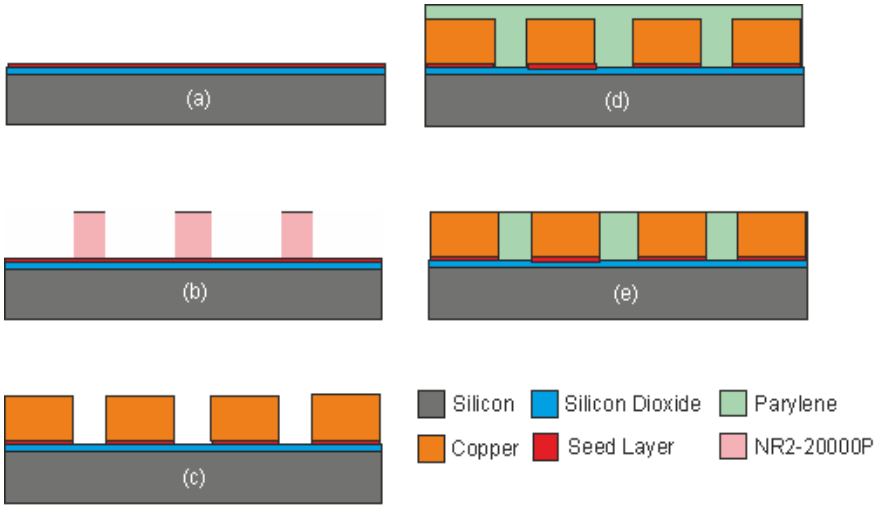


Figure 3.5: *Process sequence for the test chip to evaluate Parylene fill and CMP fabrication process.*

3.4.3 Parylene Fill Efficiency

The copper tracks have widths varying between 10µm to 50µm, while the trench widths between tracks vary from 2µm to 50µm. These were cross-sectioned by dicing and then the sample's cross-section was polished. A SEM cross-section of the copper

tracks with a 1:3 aspect ratio trench is presented in figure 3.6. It is clear from this figure that the trench between the 30µm copper tracks has been completely filled with Paryelne. However, the highlighted areas on this figure suggest that there has been smearing of material as a result of the polishing process. For this reason a focussed ion beam (FIB), cross-section was subsequently prepared. Figure 3.7 presents the FIB cross-sections of the copper tracks with (a) positive and (b) negative sidewalls. Negative sidewalls were the result of electroplating following a lithography process that had not been optimised. It is clear that in both cases the sidewalls have been conformally coated with Parylene. It can be observed that in the case of negative sidewalls a void has formed. However, as Parylene is deposited under vacuum (0.1Torr), and as no corrosive or solvent chemistry is involved in the deposition process (as detailed in section 3.2), it is thought that this void would probably be relatively benign. It is clear that Parylene deposited onto positive sidewalls has conformally coated and filled the gap between the copper tracks, with a seam where the Parylene joined. Hence, positive sidewalls should be employed to avoid the occurrence of voids between tracks.

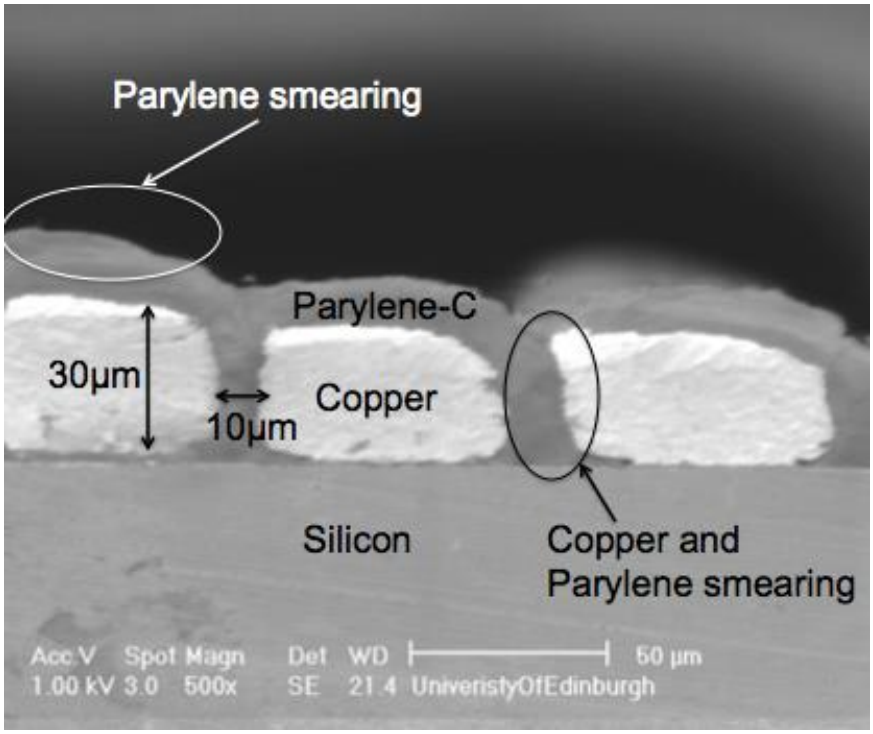


Figure 3.6: *SEM cross-section of copper tracks coated with Parylene prepared by dicing and subsequent polishing of the cross-section.*

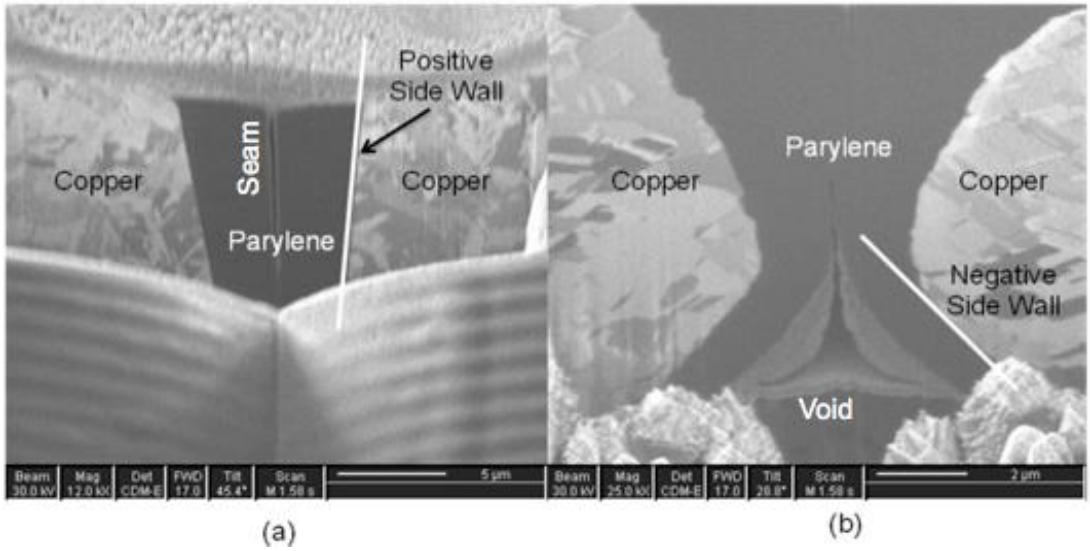


Figure 3.7: *FIB cross section of copper tracks with (a) positive and (b) negative sidewalls, conformally coated with Parylene.*

3.4.4 Chemical Mechanical Polishing of Parylene

The chemical mechanical polishing of Parylene is a process that has not been detailed in literature, and hence no details were available concerning the most appropriate slurry to use. Klebosol 30HB50 with custom additives was selected as it had previously been successfully used for CMP of SU-8. A schematic diagram of the CMP setup are presented in figure 3.8 and the parameters used for the successful CMP of Parylene were as follows: back pressure – 0.4Bar; down force – 0.17Bar; pressure on wafer – 0.25Bar; platen speed – 30RPM; wafer speed – 35RPM; polishing time – 2min.

The CMP of Parylene was first carried out on planar silicon wafers with a 5µm blanket layer of deposited Parylene. AFM measurements of Parylene before and after CMP, as presented in figure 3.9 (a) and (b) respectively, indicate there is very little change in the average surface roughness (R_a). The average surface roughness was measured to be 4.6nm and 5.5nm, before and after CMP respectively.

The average removal rate of Parylene on top of the copper stripe structures was determined to be 833±33 nm/min. AFM measurements of the copper tracks and Parylene fill between tracks following CMP are presented in figure 3.9 (c), and resulted in an average Parylene surface roughness (R_a) of 7.9nm.

An evaluation of Parylene dishing between 50µm tracks, with varying separation, was carried out. The dishing profile was measured using a Dektak surface profiling tool and confirmed using AFM. A maximum dishing profile of 619±70nm was measured.

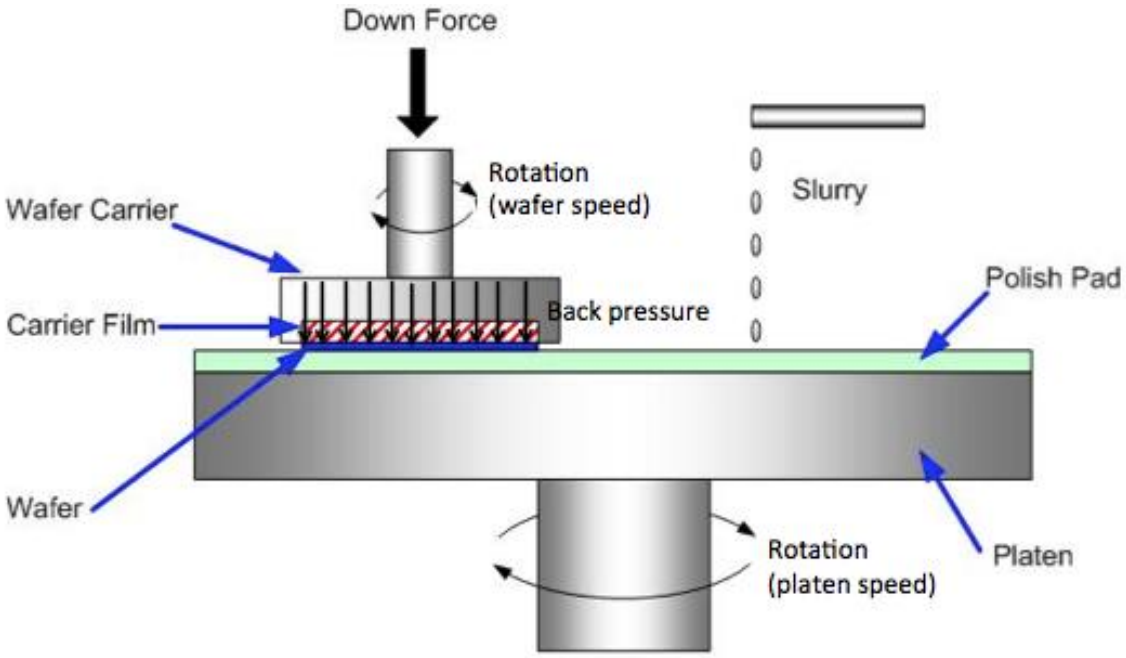


Figure 3.8: Schematic diagram of the chemical mechanical polishing tool [165].

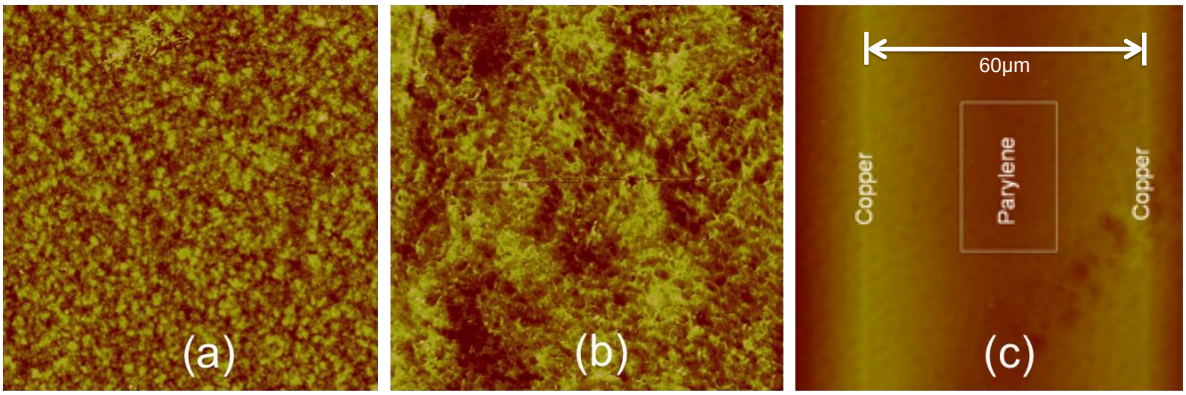


Figure 3.9: *AFM surface profiling measurements of unprocessed silicon wafer with blanket Parylene deposited (a) before CMP and (b) after CMP. (c) surface profiling of Parylene deposited on copper tracks, after CMP.*

3.5 Microinductor Characterisation

3.5.1 Microinductor Fabrication Process

In order to confirm the integration of Parylene with the proposed process architecture, the microinductor process flow (as described in section 3.3) was implemented and a schematic of the inductor cross-section is presented in figure 3.10 (a).

In order to evaluate the relationship between inductance, Q-factor and volume fraction of NiFe each mask design included a number of inductor architectures with three different degrees of NiFe encasing the copper coil. These are shown in figures 3.10 (b) to (d) with levels of encapsulation (percentage of the copper coils with NiFe core wrapped around the structure) of 52% (type 1), 82% (type 2), and 99.5% (type 3), respectively. A cross-section of the fabricated inductor, produced through dicing followed by polishing of the cross-section and photographed using optical microscopy, is presented in figure 3.10 (e). This cross-section confirms the gaps between copper coils have been completely filled with Parylene; NiFe is "wrapped around" the copper coils and a small magnetic gap between the top and bottom NiFe layers is visible.

Following each electroplating step, X-Ray fluorescence (XRF) measurements of the NiFe composition were taken at a similar point on all of the cores. The average composition was measured to be 22.2% Fe. This value is close to $Ni_{79}Fe_{21}$, which has been reported to produce an optimum value of permeability [100].

3.5.2 NiFe Electroplating Process

As was discussed in chapter 2, the NiFe electroplating bath setup plays a major role in defining the permeability of the electroplated NiFe [166]. The bath composition used for the electroplating of NiFe was set to be the same as that used in [136]. This composition is detailed in table 2.2, and the pictures of the bath setup and wafer holder are presented in figure 3.11. With this setup the electrolyte is agitated using a pump, which creates a jet stream of electrolyte onto the surface of the wafer. In addition, the bath chemistry has been optimised to produce $Ni_{80}Fe_{20}$ when the current density is $10mAcm^{-2}$.

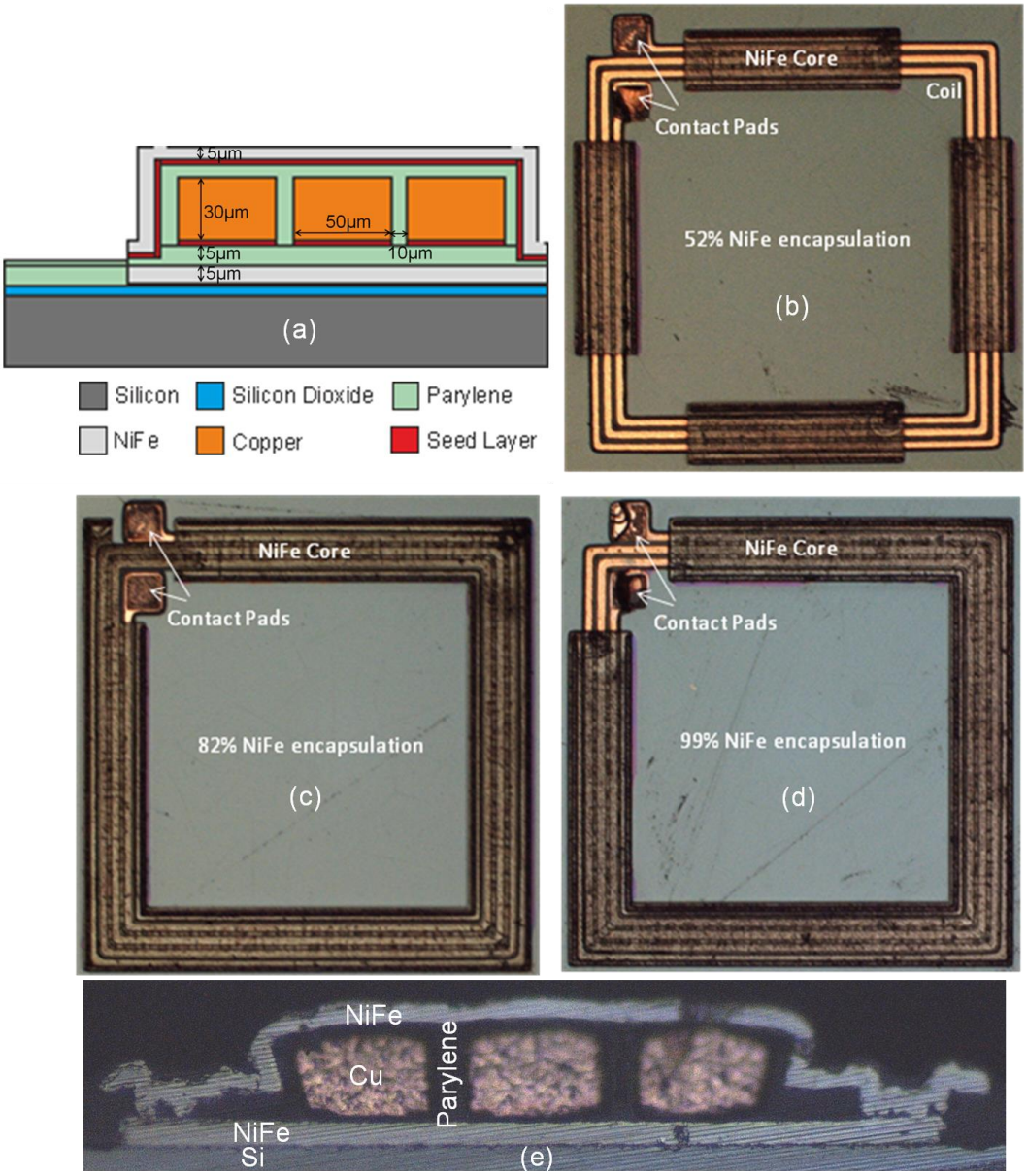


Figure 3.10: *(a) schematic cross-section of inductors cross-section; Top down view of type 1 (b); type 2(c) and type 3(d) inductors. (e) cross-section of fabricated inductor.*

3.5.3 DC Measurements of Coil Structures

The 3 turn coils have a track width of 50µm, and separation between windings of 10µm (pitch of 60µm). DC electrical measurements on these coils when coated with 5µm of Parylene are presented in Figure 3.12. Measurements were carried out using a HP4156B Precision Semiconductor Parametric Analyser and the values of resistance obtained were 1.86 ± 0.04 Ω. These results

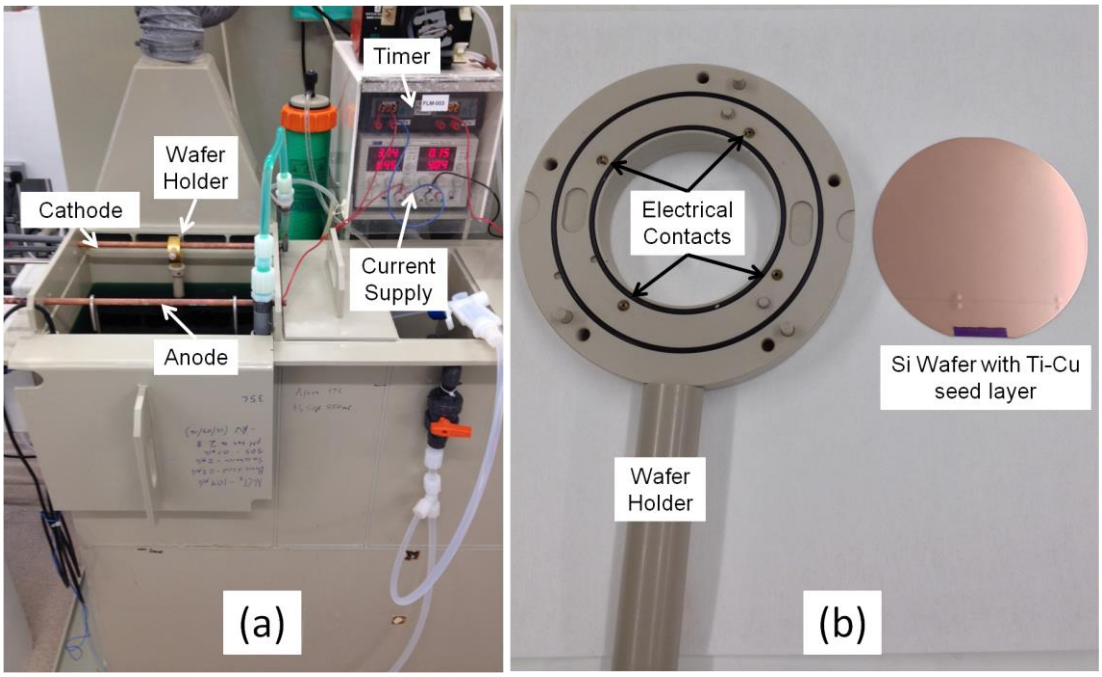


Figure 3.11: *(a) Electroplating bath setup, showing anode and wafer loaded into the bath, and (b) wafer holder.*

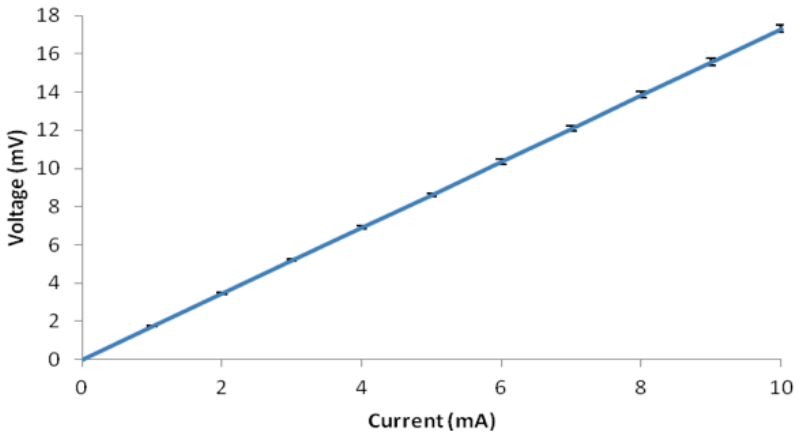


Figure 3.12: *Voltage-current measurements of microinductor coil, error bars indicate standard deviation.*

Confirm that the seed layer between windings has been completely removed by chemical etching and also confirms Parylene's suitability as an inter-coil insulator.

3.5.4 Inductance and Q-Factor Spectra

Fully operational planar spiral microinductors, as presented in figure 3.10, have been characterised using an HP4275A LCR over the 100kHz to 10MHz range. Inductance and Q-factor spectra are presented in figure 3.13. As was discussed in chapter 2, the

Q-factor is the result of DC and AC resistive losses, core eddy current losses and core magnetic hysteresis losses. It is well understood that there is a correlation between volume fraction of NiFe in the inductors core and measured inductance value. Hence, those with the highest volume fraction of NiFe (type 3) produce the highest inductance value, (130nH at 10MHz). However, this architecture incorporates a continuous NiFe core which results in higher eddy current losses and subsequently the lowest measured Q-factor of 1.9, at 10MHz.

Consequently, architectures with 52% NiFe encapsulation produced the lowest inductance values (114nH) whilst producing the highest Q-factor (2.9 at 10MHz). For this architecture, the core only encapsulates four sections of the coil. Therefore, eddy currents are constrained to these areas, resulting in significantly less eddy current losses than with type 3 architectures.

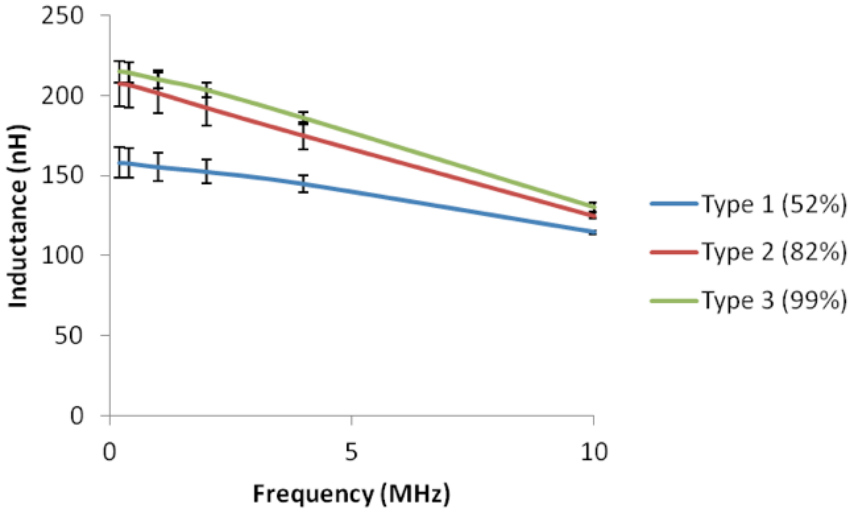
These results clearly highlight the relationship between volume fraction of NiFe and Q-factor. Therefore, in order to develop high Q-factor and high volume fraction magnetic core inductors, eddy currents must be constrained. Typically this is implemented by laminating the core inductor as has been presented by many inductors reported in literature [148, 167, 168]. Alternatively, the current path can be broken by patterning the magnetic core, as will be discussed in chapter 6.

3.6 Conclusion

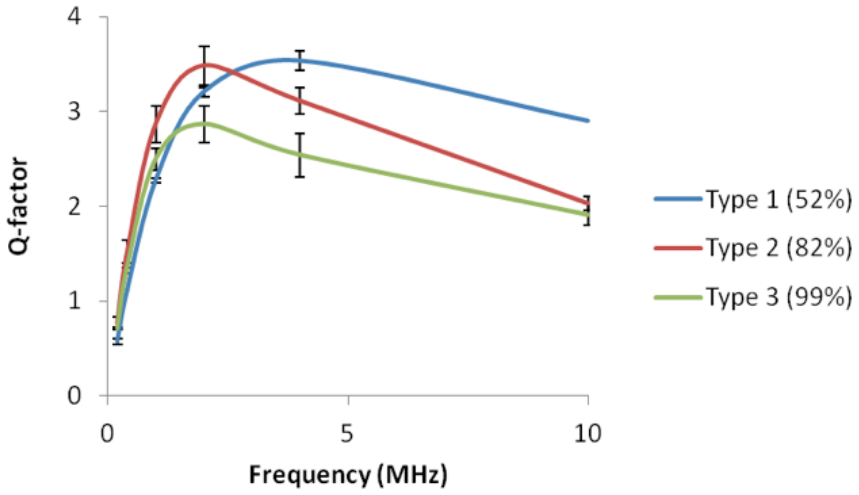
This work has characterised Parylene and demonstrated that this material can be successfully used to fabricate planar spiral microinductors with thick electroplated copper coils and NiFe alloy cores.

Good adhesion between Parylene and all layers tested has been demonstrated by employing Scotch tape tests. In addition, Parylene fill performance has been evaluated and it has been demonstrated that Parylene can completely fill 3:1 aspect ratios. It has been shown that the formation of void-free deposition can be achieved when depositing Parylene onto structure with positive sidewalls.

A successful CMP process for the polishing of Parylene on top of thick copper structures has been developed and demonstrated a high removal rate of 833±33nm/min, and an average surface roughness after polishing of 7.9nm, between



(a)



(b)

Figure 3.13: *(a) Inductance and (b) Q-factor spectra for fabricated planar spiral microinductors, error bars indicated standard deviation.*

the thick copper tracks. The evidence of excellent compatibility of Parylene with other intrinsic materials and processes has been confirmed by the successful fabrication of a fully operational microinductor. This microinductor incorporates Parylene as an insulating and structural layer, and to date has not exhibited any delamination that is often experienced with SU-8Inductors that incorporate SU-8 as a dielectric layer require a maximum processing temperature of 200˚C, as a result of SU-8 hard baking process. The inductors fabricated in this work reduce the maximum processing temperature to 140˚C. This is thought to reduce the stress in the NiFe core [169, 170]

Electrical results show that fabricated microinductors produce inductance values of 114nH, 125nH, 130nH and Q-factors of 2.9, 2.0, 1.9 for inductors with 52%, 82% and 99% NiFe encapsulation, at 10 MHz. These results confirm what would be expected where those with the highest volume fraction of NiFe produce the highest Q-factors and lowest inductance values, and those with the lowest NiFe encapsulation produce the highest Q-factors and lowest inductance values.

Chapter 4
Characterisation of Stress in Dielectric Layers

4.1 Introduction

SU-8 has been used as a structural and dielectric layer in a number of reported microinductor architectures [120, 171]. However, intrinsic problems with mechanical stress resulting from shrinkage during the cross linking process [120, 137, 171], can often affect the reliability and the total yield of the fabricated devices. For this reason, it is important to be able to characterise the stress in this material, at various processing conditions.

Chapter 3 demonstrated the suitability of Parylene-C as a structural and dielectric layer in planar spiral microinductors. However, as residual film stress, in the dielectric layers, have been linked to the reliability of the inductor [172, 173] it is necessary to characterise the stress in Parylene-C films. Parylene has presented no issues with adhesion (table 3.1), and is expected to produce low stress films, due to its room temperature deposition process. However, the inductor fabrication process (section 3.3) requires processing temperatures of up to 140°C (soft-bake temperature of NR2-20000P). Hence, it will be necessary to characterise the stress in Parylene films as a result of processing temperature.

Additionally, chapter 3 demonstrated the suitability of Parylene as a replacement for SU-8 as a structural and dielectric layer. Hence, the residual stress in SU-8 5 and 3005 will be characterised for comparison with Parylene.

4.2 Stress Measurement

Typically, the residual stress in films deposited onto silicon wafers is determined by measuring the curvature of the wafer, and calculating the film stress (σ_f) using the Stoney formula [132, 133], as presented in chapter 2.

Dabral [174] used the wafer curvature method to determine the stress in Parylene-N films, under vacuum (50-200mTorr), using a range of annealing temperatures. Stress was observed to decrease from 20MPa compressive (after deposition), and become tensile with increasing annealing temperature with a maximum stress of 53MPa at

250°C. Additionally, Hsu [175] measured the stress in Parylene-C using the wafer curvature method. Following deposition the stress was measured to be 1.56MPa.

However, the wafer curvature method relies on the assumption that film is homogenous and isotropic [132], which may not be the case as result of impurities in the film [176]. This method also requires literature values of Young's modulus and assumes that film and substrate thickness are uniform. Clearly, a method that would allow for local measurements of residual stress and Young's modulus would resolve these issues.

Another popular method of measuring stress in films is the load deflection technique. This technique requires membrane test structures to be fabricated using the material of interest. A known pressure differential is applied between the two surfaces of the membrane, and the deflection of the centre of the membrane measured. Equation 4.1 relates the pressure differential (p), to the film stress (σ_f), Young's modulus (E) and Poisson's ratio (v), for circular membranes [176]:

$$p = \frac{4t_s\sigma_f}{r^2}h + \frac{8t_s}{3r^3}\frac{E}{(1-v)}h^3 \tag{4.1}$$

where t_s, r, and h are the film thickness, membrane radius and displacement of the centre of the membrane, respectively. The attraction of this technique is that it allows for the simultaneous measurement of stress and Young's modulus. However, it suffers from the need for complex measuring equipment such as interferometry and highly accurate air pressure regulator systems.

Xing [177] and Chi-Yuan [144] employed the load deflection method and found the residual stress, Young's modulus and yield strength of Parylene-C to be 20.88MPa, 4.48GPa and 59MPa, respectively. Furthermore, load deflection membranes and strain indicator structures have been utilised in [178] to characterise strain in thin (0.5µm) Parylene-C films. This study determined the stress to increase from 21MPa to 51MPa tensile, when increasing annealing temperature from 100°C to 180°C, and found that 90% of residual stress developed in Parylene was attributed to thermal stress.

Most recently, Jyan-Siang [146] has determined residual stress by measuring the deflection of bilayer silicon-Parylene microcantilevers, measured using vertical

scanning interferometry. The residual stress was measured to be 8.2MPa, after deposition.

The automated wafer mapping of strain indicator structures, as described in [37, 136, 137, 179, 180] has been used to characterise spatial strain variation in copper, NiFe and 35µm thick SU-8 3035 films across the surface of an eight-inch wafer. The characterisation method outlined involves fabricating up to 12,288 suspended strain indictor structures on an eight-inch wafer. Measurements were carried out using the Cartesian stage on a Suss Microtech PA200 semi-automatic prober, and capturing images of the test structures using a computer based Labview system. However, these studies did not determine stress from the measured strain value, as a local value of Young's modulus was not available.

Schiavone [37] has developed a process that determines the spatial variation in stress of NiFe films. This technique combines wafer maps of strain and Young's modulus, determined using independent measurements of strain indicator structures and nanoindentation, respectively. This process will be applied in this chapter for the characterisation of dielectric layers.

This study reports on the characterisation of the residual stress in 5µm thick SU-8 and Parylene-C films as a result of process parameter variation. Measurements include the spatial variation of strain, mapped over the surface of three-inch wafers. This involves measuring an array of 720 micro-fabricated rotating pointer arm test structures. Stress is derived from localised measurements of strain and Young's modulus [37].

4.3 Test Structure Design

The mechanical test structures used in this study consist of a rotating pointer arm structure, and two lateral expansion arms. The expansion arms are offset at the point where they connect to the pointer arm. Thus, expansion or contraction in these arms results in rotation of the pointer arm in the plane of the layer. Figure 4.1 shows a schematic of the test structure, which has been reported previously [39, 136, 181]. In this design clockwise rotation indicates a tensile residual stress, whilst counter clockwise rotation indicates a compressive residual stress.

Rotation of the pointer arm is therefore a measure of the strain in the expansion arms, defined as:

$$\varepsilon = \frac{\Delta l}{l_0} \tag{4.2}$$

where Δl is the change in length of the expansion arm and l_0 is the original design length of the arm. Stress (σ_f) is related to strain through the equation:

$$\sigma_f = E\varepsilon \tag{4.3}$$

where E is the Young's modulus of the film.

Maximum rotation has been found previously to occur when the ratio between the expansion arm's offset and width is ~1.5 . However, when characterising strain in films with low Young's modulus (<10 GPa) it is advantageous to increase this ratio to 2 in order to reduce the maximum degree of rotation, and hence the local stress, due to local bending, at the point where the expansion arm connects to the pointer arm [37].

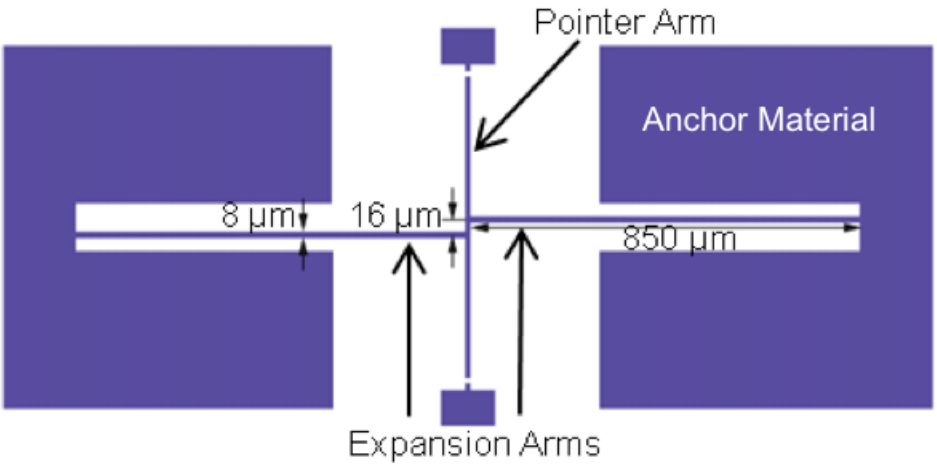


Figure 4.1: *Schematic of strain test structure.*

4.4 Fabrication

The fabrication processes for Parylene and SU-8 strain indicator structures are presented in figure 4.2. The SU-8 deposition, lithography and thermal treatment processes have been adapted from the process used to develop the National Semiconductor inductor, discussed in chapter 2.

For Parylene strain structures the process is as follows:

(a) 700nm of polysilicon is LPCVD deposited on a silicon wafer; this will act as a sacrificial layer.

(b) 5µm of Parylene is then deposited.

(c) SPR 220-7 is spin coated to a thickness of 7μm and pattered to form an etching mask for the Parylene. The Parylene layer is then etched using an RIE based oxygen plasma process to create the strain indicator structure pattern. Following etching, SPR 220-7 was stripped. It was at this point that thermal processing was carried out on the wafer. Parylene wafers were heated to temperatures of 70˚C, 140˚C, and 200˚C to investigate the effect of thermal budget on the film's residual stress.

(d) Following thermal treatment, the strain indicator structures were released by isotropically etching the polysilicon sacrificial layer using Memsstar Orbis 1000 XeF_2 vapour etch tool.

Two types of SU-8 (SU-8 5 and SU-8 3005) were considered in this study, and the process used to fabricate and release the strain indicator structures is described as follows:

(a) 700nm of polysilicon is LPCVD deposited on a silicon wafer.

(b) SU-8 was spin coated to a thickness of 5μm.

(c) SU-8 was then patterned to form the strain indicator structure pattern. The effect of three hard bake (HB) conditions were examined, hard baking at 200ºC, 150ºC and 200ºC with a gradual cool down to room temperature (2.83˚C/min).

(c) Again, the sacrificial polysilicon layer was etched using XeF_2 vapour to release the structures.

A released strain indictor structure, fabricated from Parylene and indicating a tensile strain is presented in figure 4.3.

4.5 Young's Modulus Measurements

Nanoindentation measurements were used to determine spatial variation in Young's modulus across three-inch wafers. The nanoindenter used was a Hysitron triboindenter with a Berkovich diamond tip, which indents into the surface of the material using a controlled force regime while measuring the response of the film. The load applied by the tip is ramped to 2mN at a rate of 0.4mN/sec, then held for 10

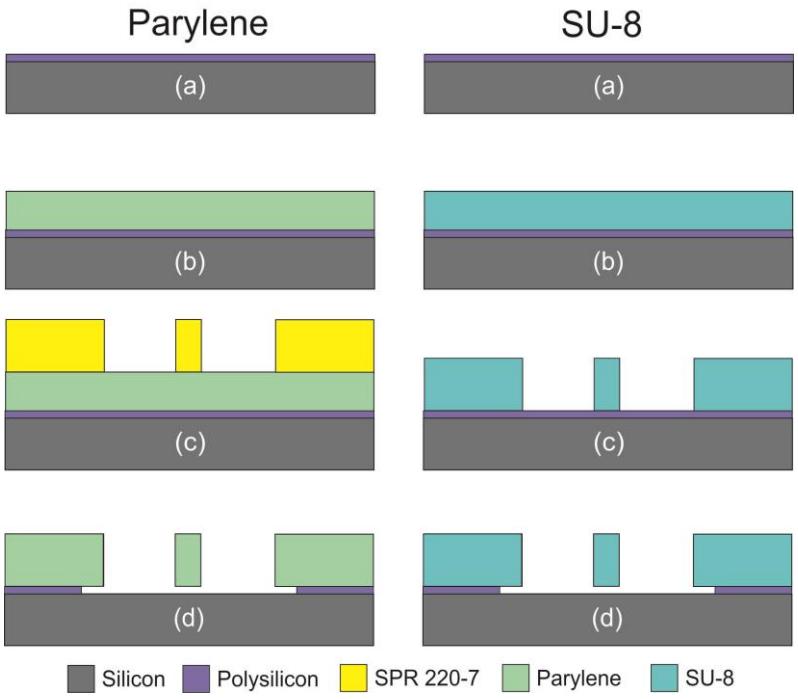


Figure 4.2: *Process Flow for Parylene and SU-8 strain indicator structures.*

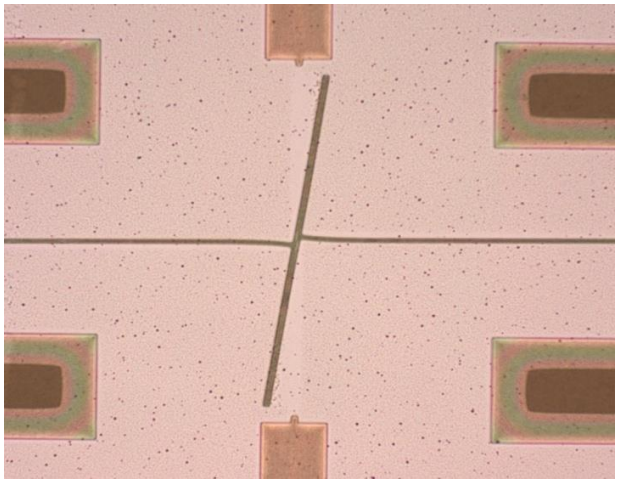


Figure 4.3: *A released Parylene strain indicator structure (note: the expansion arms are anchored out of view).*

seconds, and ramped down at a rate of 0.4mN/sec. Typical measured indentation curves for SU-8 5 and Parylene are presented in figure 4.4. The data from the unloading segment of this curve is used to extract the Young's modulus using the curve fitting procedure detailed in [182]. This technique involves the calculation of the unloading stiffness (S), which is a function of the contact area of the indenter tip (A), and subsequently a function of the penetration depth.

$$S = \beta \frac{2}{\sqrt{\pi}} E_{eff} \sqrt{A} \tag{4.4}$$

where E_{eff} is the effective Young's modulus and β is a dimensionless parameter used to account for deviations in stiffness as a result of the lack of axial symmetry. The effective Young's modulus is related to the Young's modulus of the specimen by:

$$\frac{1}{E_{eff}} = \frac{1-\nu^2}{E} + \frac{1-{\nu_i}^2}{E_i} \tag{4.5}$$

where E_i and ν_i are the Young's modulus and Poisson's ratio of the indenter tip, respectfully.

To wafer map Young's modulus, each three-inch wafer was diced into 1 cm^2 chips, and four indentation measurements were taken on each of these chips. The average Young's modulus values measured for all SU-8 and Parylene samples are presented in figure 4.5.

The measured Young's modulus values for SU-8 ranged from 4.17GPa (SU-8 3005 hard-baked at 200˚C with gradual cool down phase) to 5.49GPa (SU-8 5 hard-baked at 200˚C). In the literature, these values typically range between 3.5GPa and 7.0GPa [183], in good agreement with the values determined in this work.

Values of Young's modulus for Parylene reported in the literature range between 2GPa and 5.29GPa [184, 185]. This compares with the measured parameters in this work, which were 1.01GPa to 2.87GPa for non-annealed and annealed samples at 140˚C respectively.

4.6 Finite Element Modelling

Finite element (FE) modelling, using the ANSYS structural mechanical module, has been used to combine strain data with Young's modulus measurements, to compute values for residual stress. This FE model simulates the response of the test structure for a given stress and Young's modulus. The solution procedure has been automated through the use of ANSYS parametric design language (APDL), and outputs the rotation angle of the strain indicator structure for stresses from 0 to 100MPa, incrementing in steps of 2MPa and for Young's modulus values from 0.5GPa to 5GPa in incremental steps of 0.2GPa.

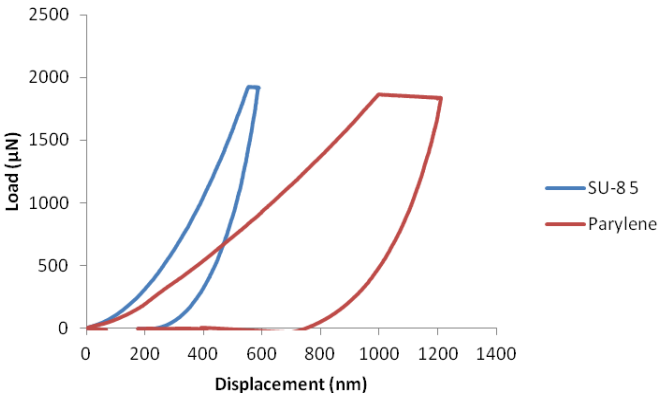
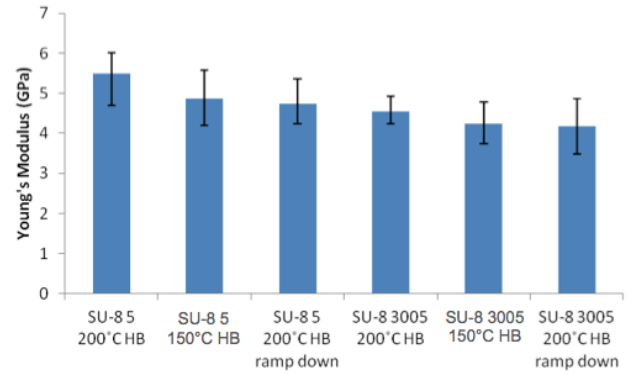
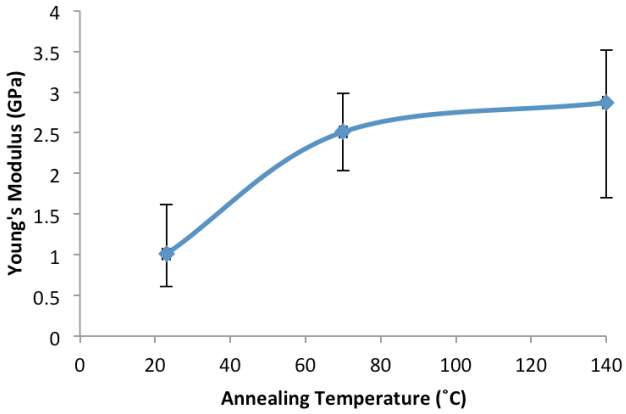


Figure 4.4: *Indentation curves for SU-8 5 hard baked at 200˚C and non-annealed Parylene.*



(a)



(b)

Figure 4.5: *Effect of annealing temperature on Young's modulus for: (a) SU-8, (b) Parylene. The error bars indicate range in both figures.*

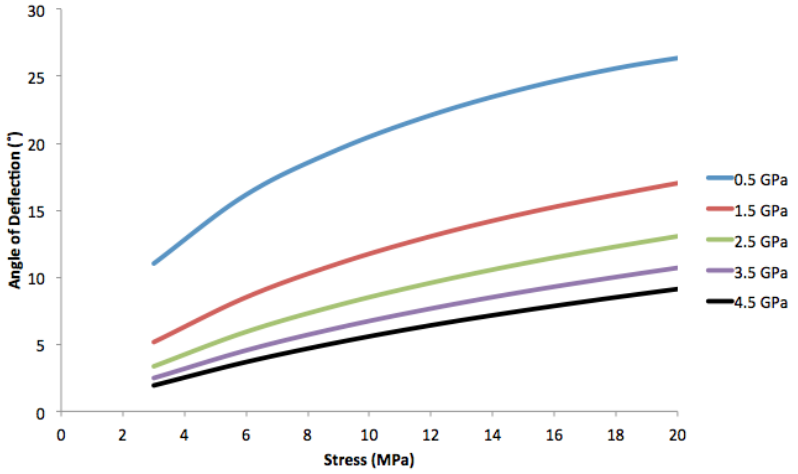


Figure 4.6: *Simulated results of residual stress mapped against angle of rotation for a range of Young's modulus values.*

The strain data obtained from the simulated curves (figure 4.6) was then correlated with strain data obtained from strain test structure measurements, in order to determine stress in the film.

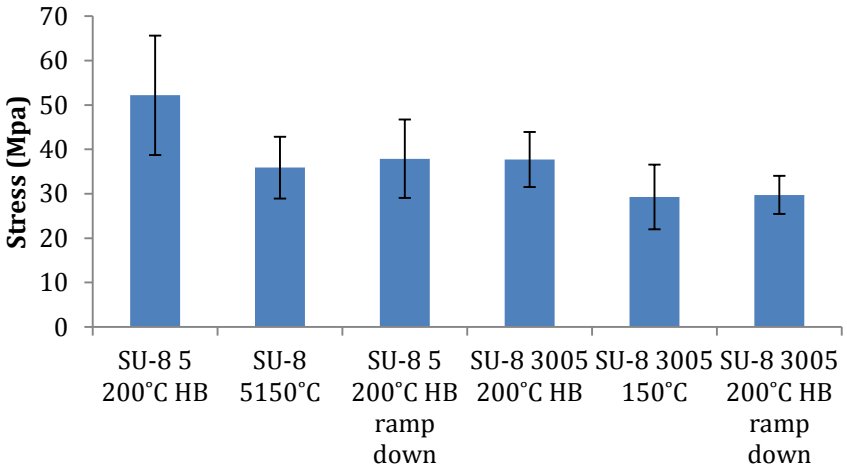
4.7 Stress Wafer Mapping

By correlating strain measurements from the pointer arm test structures with the simulated response of the strain indicator structure (figure 4.6), it has been possible to determine the stress in the Parylene and SU-8 films. Figure 4.7 presents the average stress for each of the SU-8 and Parylene films.

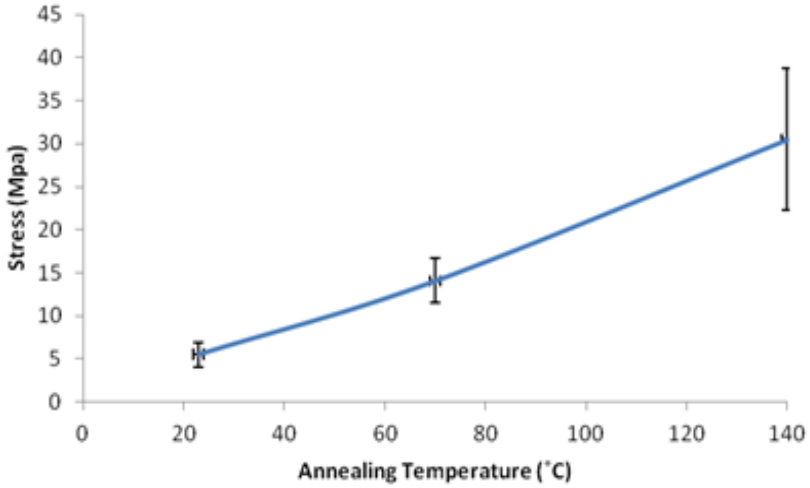
In addition, by correlating the position of strain and nanoindentation measurements on the wafer it has been possible to determine local values of stress, and subsequently wafer map strain; Young's modulus; and stress for each film. These wafer maps are presented in figure 4.8.

The degree of crosslinking in SU-8 films has been attributed to film shrinkage and subsequently residual tensile stress [180, 186]. Films hard baked at 200˚C were determined to have 44% and 30% greater stress than those hard baked at 150 ˚C, for SU-8 5 and SU-8 3005, respectively and this is attributed to a greater degree of cross linking in these films.

It is interesting to note that SU-8 films that were hard baked at 150˚C exhibited approximately the same average stress values (~36MPa for SU-8 5 and 29MPa for SU-



(a)



(b)

Figure 4.7: *Average stress data for (a) SU-8 and (b) Parylene. (error bars indicate standard deviation).*

8 3005) as SU-8 films which were hard baked at 200˚C followed by a gradual ramp down. Films that were quenched after hard baking experience thermal shock, and subsequently a higher degree of shrinkage than those that were cooled gradually. Hence, films that were cooled gradually exhibited 27% and 21% lower stress for SU-8 5 and SU-8 3005, respectively.

SU-8 3005 also exhibited a 27.7%, 18.4%, 21.5% lower average stress compared to SU-8 5 samples that had undergone the same processing conditions. This is not surprising as the SU-8 3000 data sheet states that this grade of resist has been

formulated to reduce residual stress in the film [123]. However, no details relating to how this has been achieved have been given, or are reported on in literature.

Wafer maps of SU-8 also present a large variation in stress. The worst case is with SU-8 5 for a 200˚C hard bake, where the maximum stress variation is 74MPa. This could be the result of defects in the film or non-uniform heating during thermal treatments.

As a result of the room temperature deposition process, non-annealed Parylene samples exhibit a lower residual stress than SU-8 samples (5.52 MPa), which increases to 14.07 and 30.05MPa when annealed at 70˚C and 140˚C respectively. However, it is important to note that Parylene annealed at 140°C develops a comparable level of stress with SU-8 3005 annealed at 150˚C or 200˚C followed by gradual cooling.

When Parylene is annealed at 200˚C all the stress test structures fractured during the release processing step, and it was therefore not possible to obtain any quantitative information. It is postulated that their rotation angle would be significantly larger than of those annealed at 140˚C and as a result they experienced a high degree of stress resulting in fracture. The Young's modulus of Parylene annealed at 200˚C was found to be 5.2 GPa. Therefore, a significant increase of 414% in Young's modulus between non-annealed Parylene and Parylene annealed at 200˚C suggests a significantly higher stress resulting from exposure to higher temperatures. This stress is assumed to exceed the ultimate tensile strength value for Parylene. Harder [178] reported a similar phenomenon, when heating above 180°C Parylene membrane test structures ruptured. Therefore when considering integrating Parylene-C into device architecture, thermal treatment must be carefully considered.

Wafer maps of non-annealed and annealed (at 70˚C) Parylene films appear to exhibit uniform mechanical properties. In this case the maximum variation in stress across the wafers is 10MPa and 15MPa for non-annealed and 70˚C annealed samples, respectively. Wafers that have been annealed at 140˚C present a 440% and 260% larger variation across the wafer, when compared to non-annealed and films annealed at 70˚C, respectively. A stress gradient is clearly observed across this wafer, from

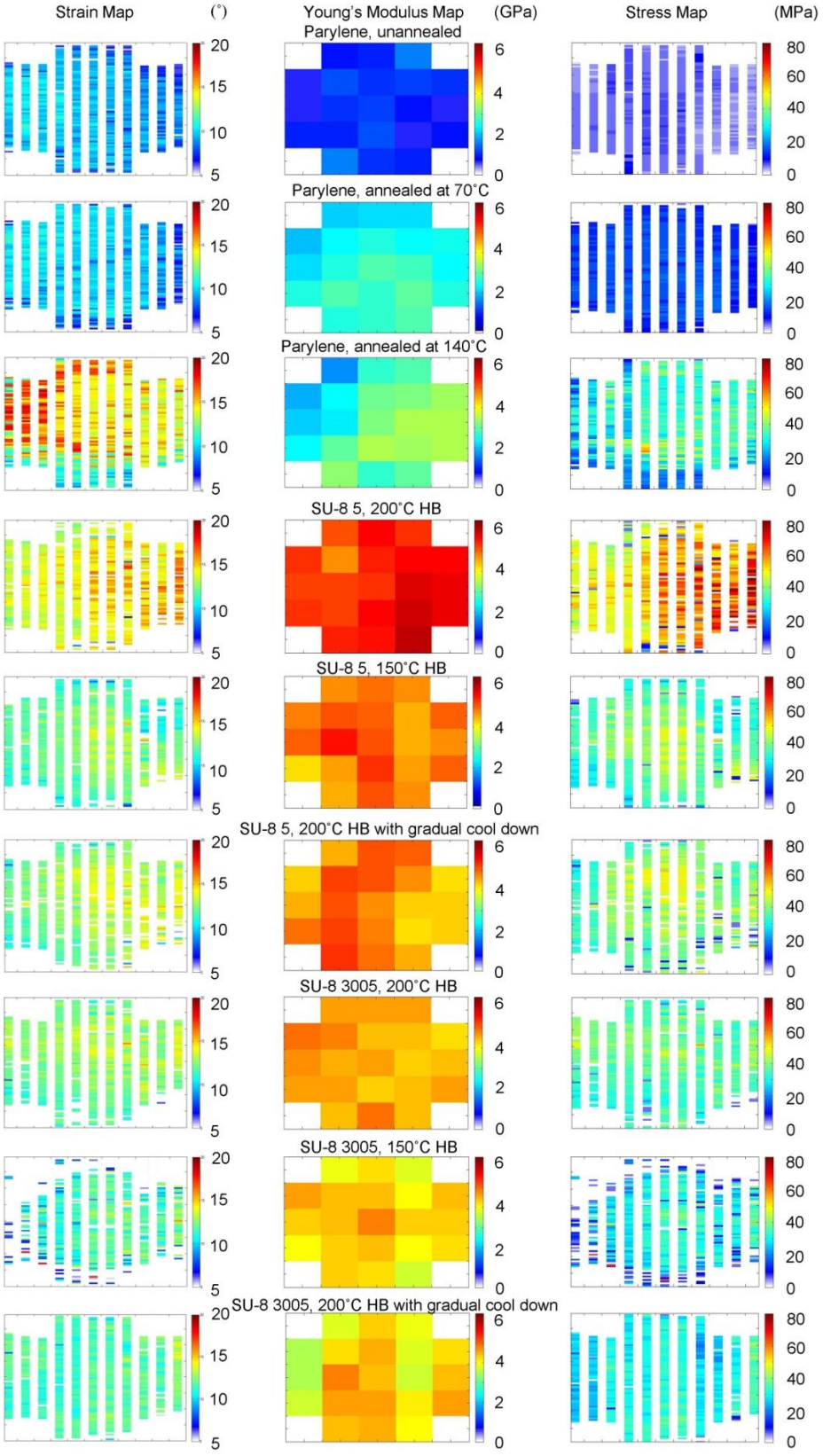


Figure 4.8: *Wafer maps of strain, Young's modulus and stress for all Parylene and SU-8 Films.*

low stress in the bottom left of the map (approximately 20 MPa) to greater levels of stress in the centre and top right of the map (approximately 40 MPa). As non-annealed and annealed at 70˚C wafers do not present a stress gradient, it is postulated that this gradient is the result of non-uniform heating.

4.8 Conclusion

In this study the strain, Young's modulus and stress have been characterised, for Parylene and SU-8 films with different thermal histories, by employing the use of strain indictor test structures and nanoindentation. By measuring the strain and Young's modulus measurements from the same position on the wafer it has been possible to wafer map strain and Young's modulus as well as the stress for each film.

It has been established that by annealing Parylene the average stress in these films increase by 116.4% and 452% for films annealed at 70˚C and 140˚C respectively. In addition, all Parylene strain indicator structures that were annealed at 200˚C fractured, indicating that the stress in the film is greater than the ultimate tensile strength of Parylene. Therefore, when considering the use of Parylene as a dielectric layer, thermal treatment must be carefully considered.

The strain, Young's modulus and stress have been characterised for two types of SU-8 (SU-8 5 and SU-8 3005) and the effect of hard bake temperature and gradual cooling on residual stress has been investigated. It is interesting to note that a gradual cool down, further to a 200˚C hard bake helped by reducing the average residual stress by 27% and 21% for SU-8 5 and SU-8 3005 respectively.

Lowering the hard bake temperature to 150˚C also reduced the average residual stress by 31% and 17%, for SU-8 5 and SU-8 3005 respectively. It is clear that these results are comparable to SU-8 samples that were hard baked at 200˚C with a gradual cool down. For samples which were annealed at 150˚C and 200˚C with a gradual cool down, it is thought that the reduced stress is the result of a lower degree of shrinkage following the hard bake stage.

SU-8 3005 samples consistently exhibited a lower stress than SU-8 5 samples (32% for SU-8 5 and SU-8 3005 samples, with 200˚C hard bake, without gradual cool down).

Chapter 5
Correlation of Magnetic, Mechanical and Electrical Properties of Electroplated Ferromagnetic Films, Studied by Automated Wafer Mapping

5.1 Introduction

Microelectronic and MEMS test structures typically consist of structures defined through lithography, and are specifically designed to aid with material characterisation and fabrication process optimisation. The attraction of using test structures is that they can be fabricated with a short turnaround time and can often be integrated with the device fabrication process to confirm wafers have been processed successfully [36]. Typically, electrical [36, 181, 187-190], optical [39, 181, 187] or physical measurements [191-193] are made on these test structures.

In the case of the microinductors, as presented in chapter 3, magnetic permeability; electrical resistivity; and residual mechanical stress properties of the electroplated NiFe core directly influence the inductance; resistive core losses; and mechanical reliability.

A number of studies have employed test structures to characterise residual stress and the electrical properties of electroplated NiFe. For example, [37] characterised stress in NiFe by combining independent measurements of strain and Young's modulus, determined through the automated wafer mapping of strain indicator structures and nanoindentation measurements, respectively. This paper reported the residual stress in NiFe increased from 50MPa to 220MPa as %Ni composition increased from 85% to 95%.

Myung [193] determined the resistivity of electrodeposited NiFe increased from 5μΩ.cm to approximately 32μΩ.cm as %Fe composition is increased from 0% to 40%. This relationship between %Fe composition and the resistive properties of NiFe was also described in [136] where the sheet resistance of NiFe Greek cross structures was characterised using automated wafer mapping.

Furthermore, the complex permeability of 100 nm thick sputtered $Ni_{81}Fe_{19}$ has been characterised over the frequency range 10MHz to 1GHz [194]. The real component of complex permeability (μ') was measured to be 2000, with ferromagnetic resonance (FMR) occurring at 0.8GHz, measured using a micro-strip bridge. Jayasekara [195], measured similar permeability values for 54nm thick sputtered NiFe films with real component permeability of 1800, measured over the same frequency range. However, 2.2μm samples measured 1200 permeability (μ') at 1MHz and the paper attributes this reduction in permeability to increased eddy current dampening, as a result of increased film thickness. O'Donnell [75], studied the effect of thickness on permeability in $Ni_{45}Fe_{55}$ electroplated films for microinductor applications with operational frequencies of up to 100MHz. It has been reported that for this composition, at low frequencies, the relative permeability is related to thickness (t) as $\mu_r = 900t^{-0.5}$. In this case the reduction of permeability with increasing thickness is attributed to the magnetostrictive effect.

The use of test structures capable of the routine measurement of permeability using standard electrical probing has not been previously reported, and hence neither has the spatial variability of permeability been wafer mapped. The ability to perform this measurement with relatively simple electrical measurements provides an opportunity for fast feedback on the magnetic performance of Permalloy depositions, which is a capability required for process control and verification measurements. In this work automated wafer-mapping measurements are reported to identify the spatial correlation between high frequency permeability, electrical resistivity, mechanical residual strain and the chemical composition of two-component permalloy film ($Ni_xFe_{(100-x)}$) electroplated on the surface of 100mm silicon wafers.

Automated wafer scale analysis is essentially required in order to:

(i) Characterise the spatial distribution of parameters over the wafer area.

(ii) Determine the optimal compromise between magnetic, electric and mechanical properties required for the particular device application.

To enable these parameters to be characterised on a single wafer a test chip was designed and the layout is presented in Figure 5.1. This test chip contains MEMS-based strain structures, high frequency permeability test structures and Greek cross

electrical test structures. This layout is designed in order to perform DC electrical, RF and opto-mechanical measurements on a single wafer. Therefore, it contains a rich variety of electrical structures and MEMS-based strain indicators. Automated test routines for measuring the test structures have been implemented using NI LabVIEW programming; a Karl Suss semi-automated wafer prober; digital camera; RF Cascade probe station and Agilent Impedance/Material Analyser E4991A (1MHz-3GHz). The resulting wafer maps of the extracted physical properties were generated using Matlab code.

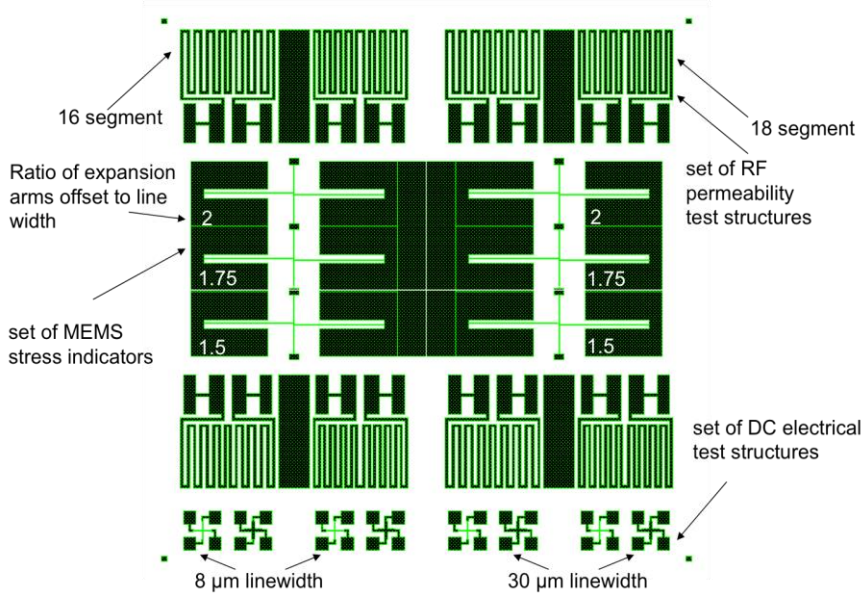


Figure 5.1: *Test chip layout, containing RF permeability; DC electrical (sheet resistance); and MEMS strain indicator test structures*

5.2 Fabrication

The fabrication process used to produce the NiFe test structures is based upon a UV-LIGA (lithography, electroplating and molding) type process, followed by isotropic etching to undercut and release the strain indicator structures. The fabrication process is presented in Figure 5.2, and a description of these steps is as follows:

(a) 700nm of PECVD silicon dioxide is deposited onto a silicon wafer, which will act as an insulating layer between the silicon substrate and the NiFe layer. Following electrical testing this layer will act as a sacrificial layer to release the strain indicator structures.

(b) Next, Ti(30nm)-Ni(150nm)-Ti(30nm) seed layer is sputtered. Following this, SPR 220-7 photoresist is spin coated to a thickness of 17 µm.

(c) The SPR 220-7 is patterned to form the mould for electroplating NiFe.

(d) The top Ti layer is etched and NiFe is electroplated to a target thickness of 16 µm.

(e) The photoresist is stripped, and the seed layer is etched using an Ar milling process. Following measurements of composition, thickness and electrical properties, an isotropic hydrofluoric acid vapour etch is used to release the strain indicator structures.

Examples of fabricated permeability test structures and Greek cross structures are presented in figure 5.3 (a) and (b), where (c) and (d) present images of the strain indicator structures before and after release.

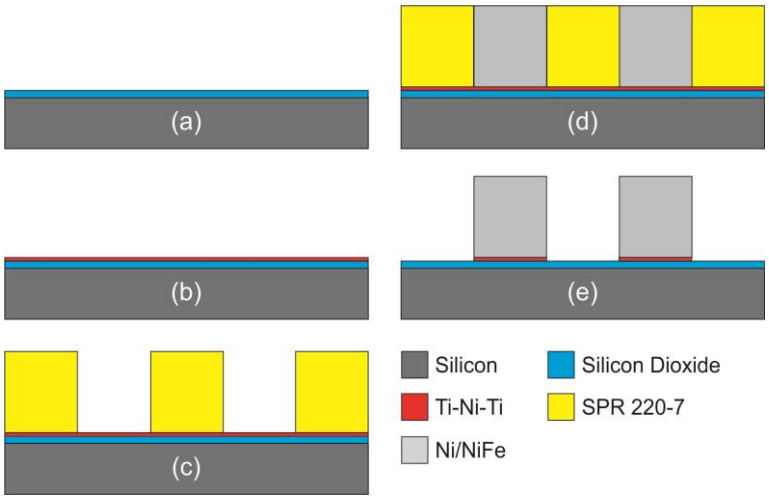
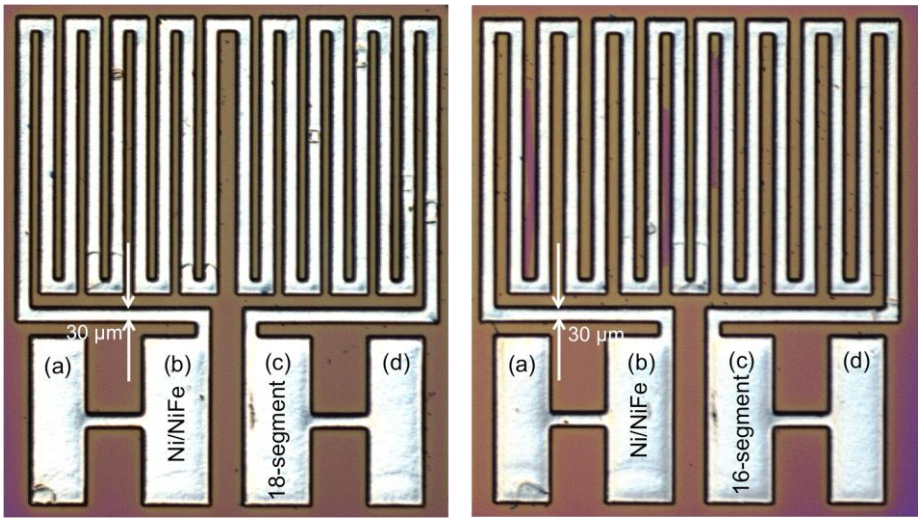


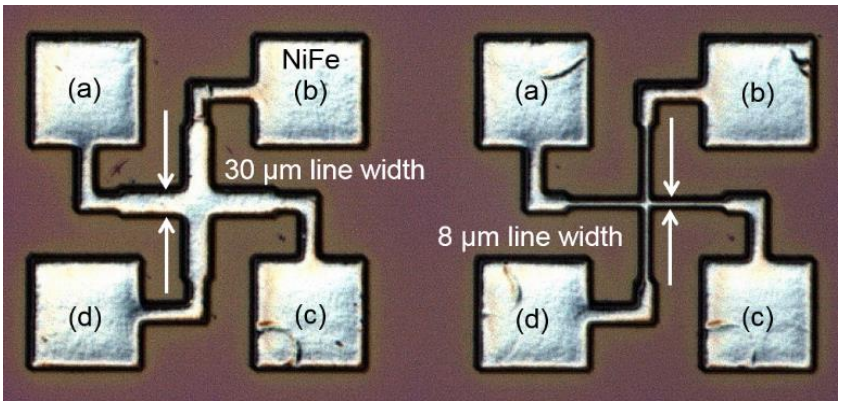
Figure 5.2: *Fabrication process for electrically characterised NiFe test structures.*

5.3 Measurements

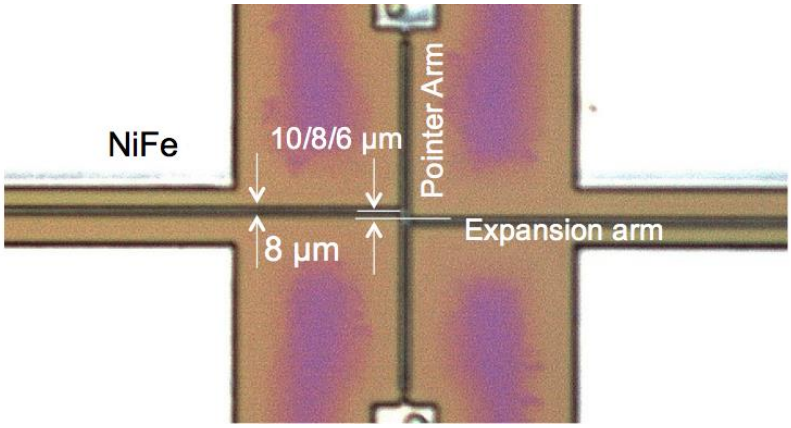
The DC resistance of the permeability test structures and sheet resistance of the Greek cross structures were measured using an Agilent 3458A digital multimeter, and current was supplied from a HP 4142B modular DC source. Standard Kelvin measurements, as described in [36, 187, 188] where current is forced from contact pads labelled (a) and (b) (figure 5.2 (b)) and voltage is measured between pads (c) and (d), were carried out on the Greek cross structures. The sheet resistance (R_s) is given by:



(a)

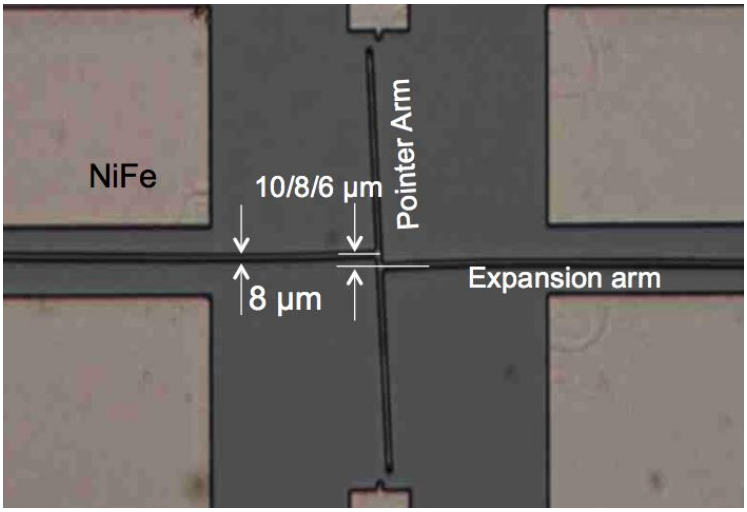


(b)



(c)

Figure 5.3: *Fabricated Ni test structures (a) 16 and 18 segment RF permeability test structures; (b) Greek cross test structures (8µm and 30µm line width); (c) unreleased strain test structure*



(d)

Figure 5.3: *Fabricated Ni test structures (d) released strain test structure (note expansion arms are mechanically anchored out of shot).*

$$R_s = \frac{\pi}{\ln(2)} \frac{V}{I} \tag{5.1}$$

where V and I are measured voltage and supplied current, respectively. The measurement is then repeated with current flow reversed. Following this, the current forcing terminals are then moved 90º such that current is now forced from (d) to (c) and measurements of voltage repeated as above, and an average of all four measurements taken. Using this method an accuracy of greater than 0.1% can be achieved [36].

Additionally, Kelvin measurements were carried out on the permeability test structures, where a current of 10mA was passed between pads labelled (a) and (d) on figure 5.2 (a), and voltage was measured across pads (b) and (c). Strain indicator structures were measured using the same process and set-up described in chapter 4.

As was discussed in chapter 2, a low frequency alternating current will flow throughout the conductor's entire cross-section, However, as frequency is increased, an increasing magnetic field, at the centre of the conductor's cross-section, results in an impedance to the current and the redistribution of current density to the edges of the conductor. This distribution of current density at the edge of the conductor is known as the skin effect and the depth into the conductor to which the current is constrained is known as the skin depth. Skin depth is a function of frequency, permeability and resistivity of

the conductor. The net result of the skin effect is an effective decrease in the conductive cross-section, and hence increase in relative resistance [75]. Using this principle, RF resistance spectra of the permeability test structures, measured using an Agilent E4991A impedance analyser, have been used to determine the skin depth and permeability spectra. The high frequency permeability measurements on the permeability test structures are based on skin depth, extracted from high frequency resistance measurements. Cascade ACP40-W GS probes with a pitch 150μm were landed on pads (c) and (d), and supplied a sinusoidal signal from 1MHz to 100MHz with a peak amplitude of 100mV.

The advantages of this approach are that it measures the magnetic properties of the skin depth and enables the magnetic uniformity over the wafer to be determined by spatially extracting the permeability at the frequency of interest. Its use as an RF electrical measurement means there is no need for any external electromagnet to produce a magnetic field.

The DC resistance (R_{DC}); resistance at given frequency (R_{RF}); and measured test structure thickness (t) were used to determine DC resistivity (ρ); effective area as a result of skin depth (A_δ); skin depth (δ); and subsequently, the relative permeability (μ_r) using the following equations:

$$\rho = \frac{R_{DC}\, wt}{l} \tag{5.2}$$

$$A_\delta = \frac{\rho l}{R_{RF}} \tag{5.3}$$

$$\delta = \frac{2w+2t-\sqrt{(-2w-2t)^2-16A_\delta}}{8} \tag{5.4}$$

$$\mu_r = \frac{2\rho}{\omega \mu_0 \delta} \tag{5.5}$$

where l and w are the length of the permeability structures coil and cross-section width, respectively; ω ($\omega = 2\pi f$) is the angular frequency; and μ_0 is the permeability of free space ($4\pi \times 10^{-7}\ H/m$).

Equation 5.4 is derived by considering a simple model of the skin depth to derive the expression for the effective area as a result of skin depth (A_δ). A schematic image of the resistor cross-section, which identifies the skin depth, is presented in figure 5.4.

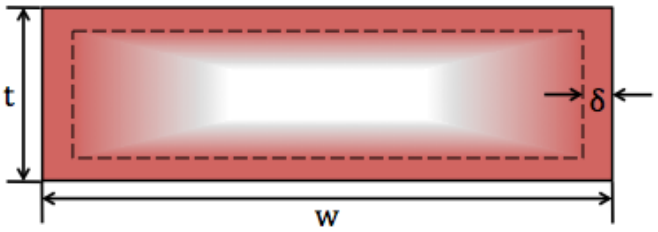


Figure 5.4: *Schematic cross-section of the permeability test structure showing the skin depth (δ).*

From figure 5.4, is it clear that the effective area as a result of skin depth can be expressed as:

$$A_\delta = -4\delta^2 + 2\omega\delta + 2t\delta \tag{5.6}$$

$$\therefore\ 4\delta^2 - (2\omega + 2t)\delta + A_\delta = 0 \tag{5.7}$$

Equation 5.4 can be derived by solving equation 5.7, using the standard quadratic root equation. This geometric approximation of skin depth area has been well documented [196]. However, more complex analytical models, such as that described in [197] could be adapted to calculate the skin depth in the permalloy test structure. Equation (5.8) [197] relates the effective resistance at high frequency (R_{RF}) to the material conductivity (σ); the electric field acting through the conductor (E_z) distribution across the conductor's rectangular cross section and (w) and (t) denote the cross-sectional width and thickness, respectively. However, [198] demonstrated that the accuracy of the geometric approximation of skin effect, used in this chapter, improves as frequency is increased.

$$R_{RF} = \frac{\int_0^t \int_{-w/2}^{w/2} |E_z(x,y)|^2 \, dx \, dy}{\sigma \left| \int_0^t \int_{-w/2}^{w/2} E_z(x,y) dx \, dy \right|^2} \tag{5.8}$$

Prior to RF measurements, hysteresis BH-loop measurements were performed on unpatterned 4µm thick $Ni_{75}Fe_{25}$ films using dedicated Shb Instruments equipment comprising of a 10Hz oscillating electromagnet and pickup coils. Figure 5.5 presents an in-plane hysteresis loop. The coercive field (H_C) defines the external field applied to a magnetic material to result in complete demagnetization, and for these films has been measured to be 40mA.m. Saturation magnetization (B_S) is the maximum possible magnetization of a ferromagnetic material; where by all of the magnetic

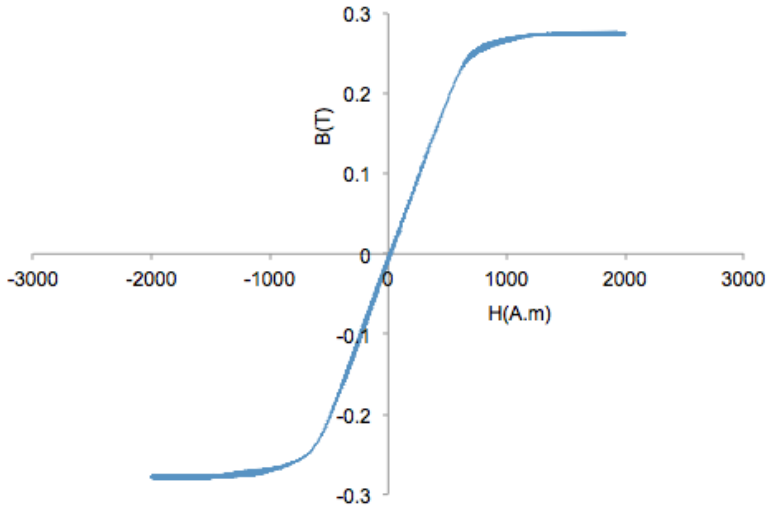


Figure 5.5: *Hysteresis (BH-loop) measured for a 5μm thick NiFe film to confirm soft magnetic behaviour.*

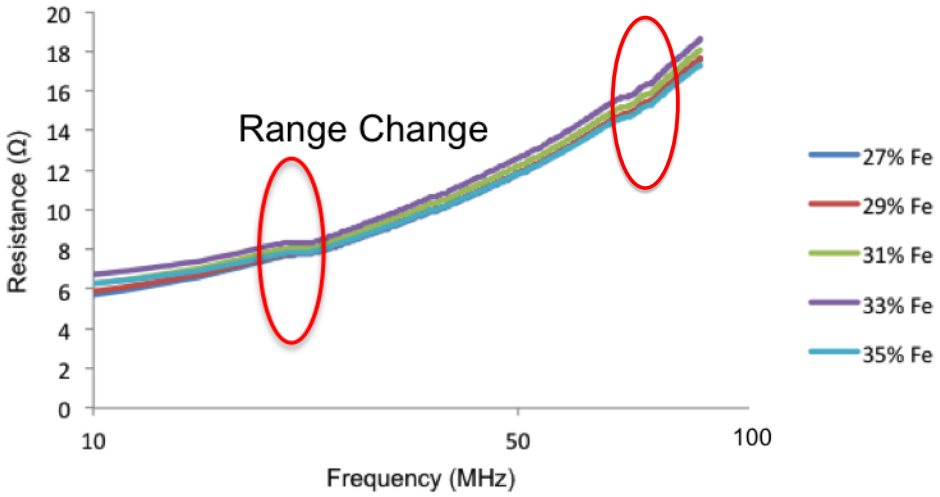
domains are aligned with the applied external field. In these NiFe films this value has been measured to be 0.25T and occurs when an external field of 750A.m is applied. This BH-loop demonstrates the very soft magnetic behaviour of these films. The hysteresis loop also shows a maximum static relative permeability of 963 when exited by 16.1A.m field. This value is in good agreement with static relative permeability values measured for other electroplated $Ni_{80}Fe_{20}$ films, which have been reported to range from 500 to 8500 [11, 110-113, 166, 194, 196, 198, 199].

Figure 5.6 presents measured values of resistance, skin depth and permeability as a function of frequency for a range of NiFe compositions (27-35% Fe). As expected, resistance increases from 5.46Ω at 1MHz to 16.81Ω at 100MHz, for 27% Fe. Two small steps in the measured resistance spectra at 20MHz and 80MHz can be observed, these are the result of range changes of the impedance analyser. These range changes have been highlighted in figure 5.6 (a).

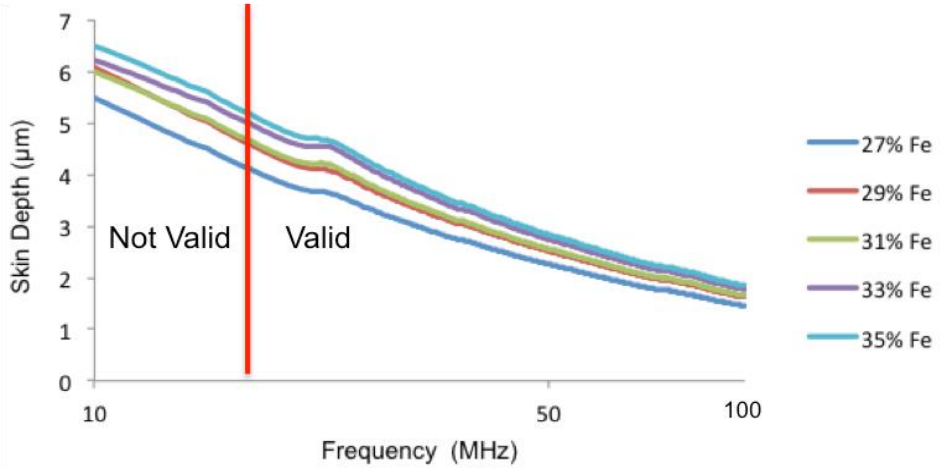
As this method relies upon the skin depth effect, then it is clear that for the skin depth model to be valid 2δ must be less than the cross-sectional thickness (t). Therefore, below 15MHz the skin depth model does not hold and the current flows through the entire permeability test structure cross-sections. Hence, below this frequency, calculations of skin depth and permeability are not valid, as indicated on figures 5.6 (b) and (c). Above 15MHz a linear dependence between %Fe composition, skin depth and permeability is observed.

There is no linear dependence on resistance with %Fe, as resistance is dependent upon the test structure thickness and material resistivity.

This methodology for permeability extraction is of particular interest, as this is the first time this parameter has been spatially extracted on-wafer using electrical measurements.

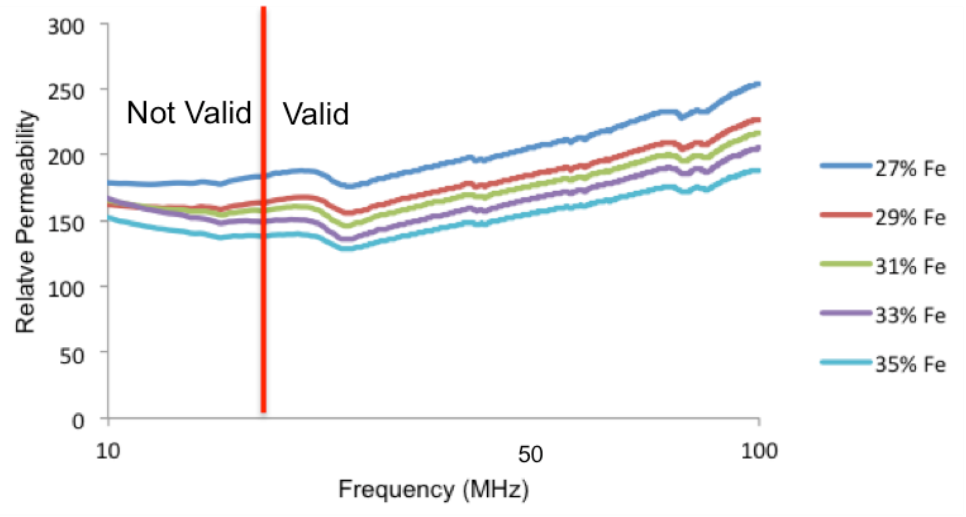


(a)



(b)

Figure 5.6: *Typical (a) resistance and (b) skin depth spectra for 16 and 18 segment resistors fabricated from 27% to 35% Fe.*



(c)

Figure 5.6: *Typical (c) permeability spectra for 16 and 18 segment resistors fabricated from 27% to 35% Fe.*

5.4 Wafer Maps

5.4.1 Electrical and Magnetic Wafer Maps

The compositional and thickness uniformity of the electroplated NiFe was wafer mapped using a ThermoFisher MXR XRF tool and Dektac surface profiler, respectively. The wafer maps shown in figures 5.7, 5.8 and 5.9 present examples of data extracted from the test structures, with 448 electrical, thickness and composition measurements were taken across the four-inch wafer.

From figure 5.7, the compositional and thickness wafer maps present different spatial variations of thickness and composition. The thickness map shows a bull's eye variation and the compositional mapping exhibiting the highest Ni content at the top right hand side of the wafer and the lowest values at the bottom left hand edge. The bull's eye is almost certainly the result of current crowding at the edges of the wafer, which results in a greater thickness at the wafer edge than in the centre. In this case electroplated thickness ranges from 14.9 to 19µm. However, variation in %Fe composition across the wafer is known to be the result of the jet agitation method used in this electroplating bath. It has been reported that the highest %Fe composition will correspond to the location of the greatest electrolyte flow rate on the wafers surface [88, 112]. A schematic diagram of the electroplating bath setup is presented in figure

5.10, which shows the position of the electrodes; agitation jet nozzle; and electrolyte flow onto the wafer. A jet agitation setup has been used in this study purposefully to produce wafers with large variation in %Fe composition.

Inspection of wafer maps presented in figure 5.7 indicate that, as would be expected, there is a correlation between the resistive and thickness measurements, this is borne out by the correlation coefficients presented in table 5.1, Correlation coefficient values of ~0.9 for skin depth and permeability with %Fe have been calculated. Table 5.2 presents the correlation coefficient of skin depth and permeability at 15MHz, 20MHz and 100MHz with composition (%Fe).

Correlation coefficients presented in tables 5.1 and 5.2 represents the Pearson product-moment correlation coefficient(r). This value characterises the linear association between two data sets (x and y), and is given by:

$$r = \frac{\sum(x-\bar{x})\,(y-\bar{y})}{\sqrt{\sum(x-\bar{x})^2\ \sum(y-\bar{y})^2}} \tag{5.9}$$

where $\bar{x}$ and $\bar{y}$ represent the mean values of the x and y data sets, respectively. Correlation coefficients close to 1 represent a strong positive correlation, where as values close to -1 represent a strong negative correlation [200]. The scatter plots presented in Appendix C present the all points from each data set plotted against thickness or composition (%Fe). It is clear from these figures with that there are a strong linear association. Hence, the high correlation coefficients presented in tables 5.1 and 5.2 are not surprising.

As is clear from equation (5.2), the DC resistance is dependent upon both thickness of the test structure and material resistivity. For this reason, it is to be expected that DC resistance has correlation coefficients of 0.83 and 0.73 with thickness and %Fe composition, respectively (for 16 segment test structures).

Iron typically has resistivity of 10μΩ.cm compared with 6.99μΩ.cm for Ni. Hence, it is to be expected that the resistivity wafer maps would present a trend of increasing resistivity with %Fe, which is confirmed by the correlation coefficient of 0.91. This trend is similar to that measured by Myung [193]. However resistivity values

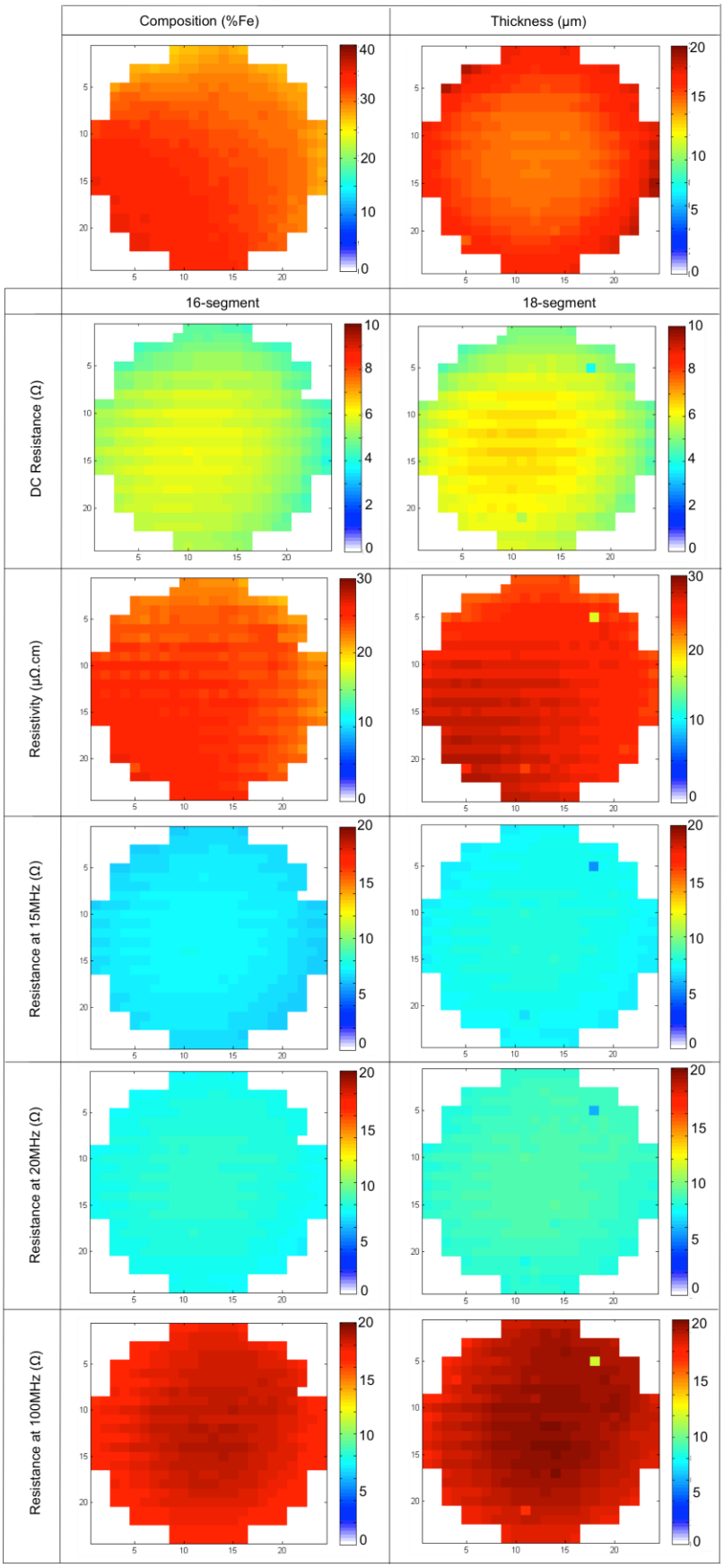


Figure 5.7: *Wafer maps of composition and thickness (top) and DC resistance, DC resistivity and resistance at 15MHz, 20MHz, and 100MHz, for permeability structures with 16 and 18 segment permeability test structures.*

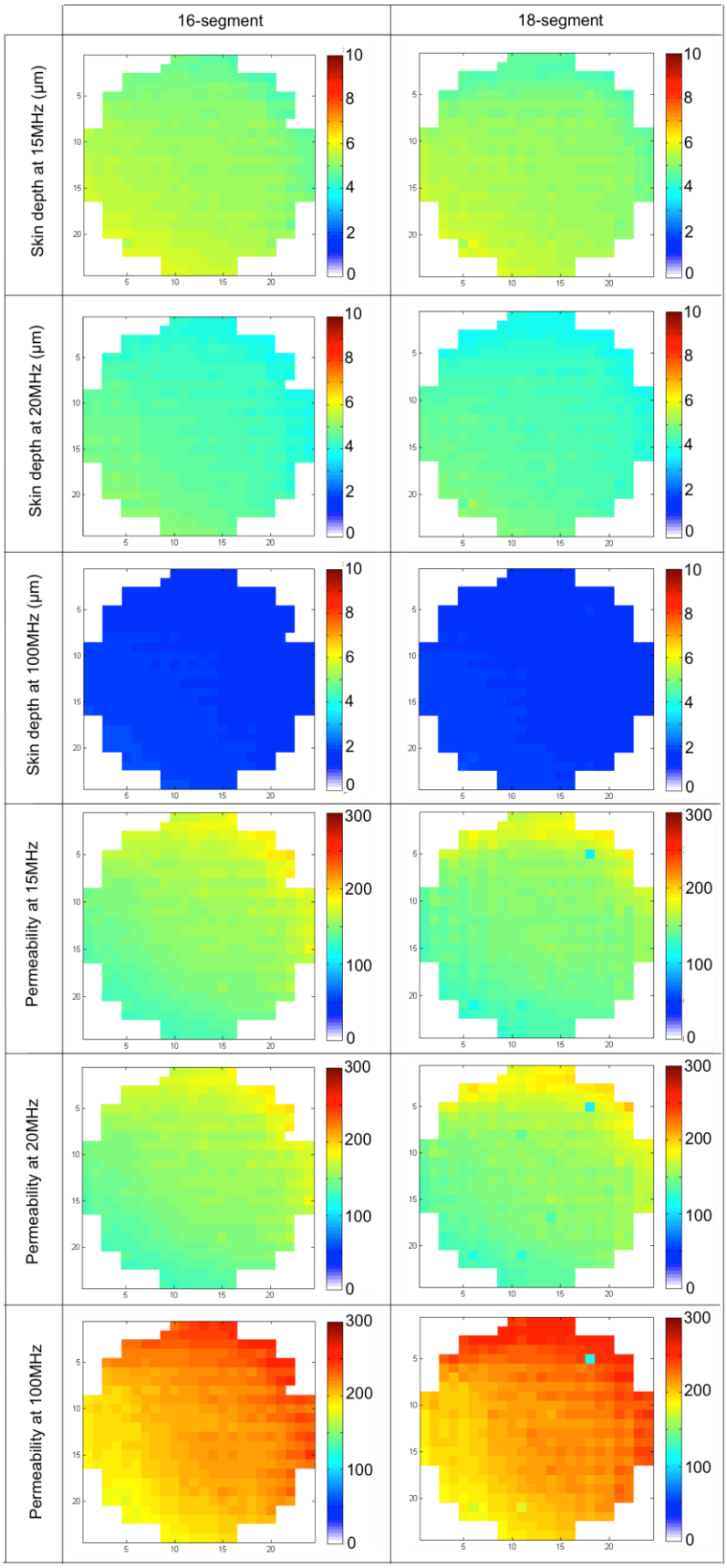


Figure 5.8: *Wafer maps of skin depth and permeability measured at frequencies of 15MHz, 20MHz, and 100MHz for 16 and 18 segment permeability structures*

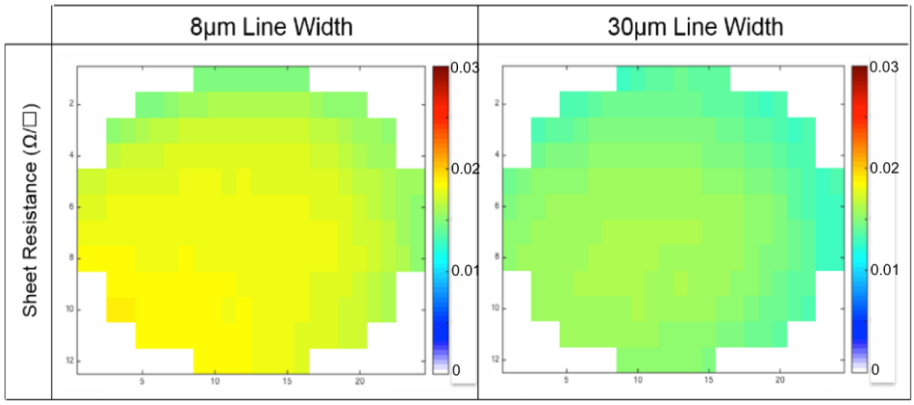


Figure 5.9: *Wafer maps of sheet resistance for Greek cross structures, with 8µm and 30µm line width.*

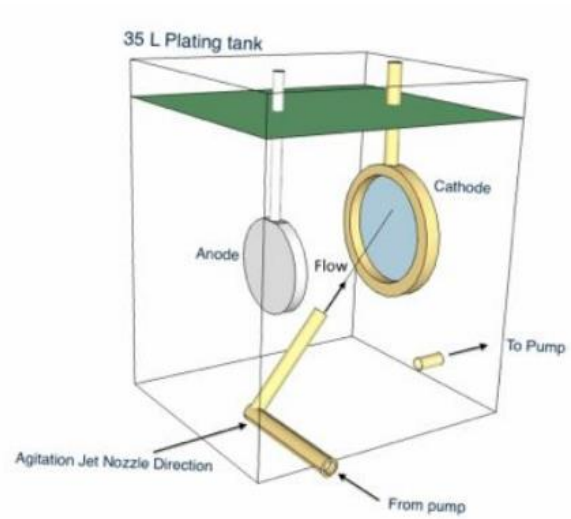


Figure 5.10: *Schematic diagram of electroplating bath setup [88].*

	Correlation Coefficient	
Correlation with Thickness	**16-segment**	**18-segment**
DC Resistance	-0.83	-0.85
Resistivity	-0.41	-0.4
Resistance at 15MHz	-0.89	-0.9
Resistance at 20MHz	-0.92	-0.88
Resistance at 100MHz	-0.87	-0.75

Table 5.1: *Correlation coefficients for thickness with resistivity, DC resistance and resistance at 15MHz, 20MHz and 100MHz.*

	Correlation Coefficient	
Composition (%Fe)	**16-segment**	**18-segment**
Skin Depth at 15MHz	0.88	0.93
Skin Depth at 20MHz	0.92	0.95
Skin Depth at 100MHz	0.91	0.93
Permeability at 15MHz	-0.78	-0.87
Permeability at 20MHz	-0.87	-0.87
Permeability at 100MHz	-0.92	-0.93

Table 5.2: *Correlation coefficient of composition (%Fe) with skin depth and permeability at 15MHz, 20MHz and 100MHz.*

measured in this work are greater than those reported by Myung. At 30% and 35% Fe, resistivity was measured to be 15μΩ.cm and 20μΩ.cm, respectively, compared to this study where resistivity at these compositions was measured to be approximately 22μΩ.cm and 25μΩ.cm, respectively. The most likely cause for the difference in these values is the electroplating bath setup, or the seed layer used. While in both cases a NiCl electrolyte was used, Myung presents no information relating to other electroplating parameters or bath setup.

Wafer maps of resistance at 15MHz show a similar pattern to the DC resistance maps. This is due to the skin depth value being comparable with half the thickness of the device, with the largest skin depth measured being 6.53μm, for 16 segment structures.

The lowest value of skin depth (1.46μm) is presented by test structures with 27.15% Fe, for 16 segment structures at 100MHz. Wafer maps presented in figure 5.8 and correlation coefficients presented in table 5.2 confirm that skin depth increases as a result of increasing %Fe. As a result of this correlation, it is postulated that this technique is more effective in NiFe films with lower %Fe. This would allow for the characterisation of permeability at lower frequencies, for films of similar thickness. This correlation, and the correlation between resistivity and Fe composition, should be considered when designing the microinductor core, as both skin depth and material resistivity would contribute to eddy current losses. This study has highlighted the relationship between resistivity and skin depth. High %Fe will allow for lower resistive

losses in the NiFe core. However, lower %Fe would enable eddy currents to be constrained to the skin of the core.

The negative correlation between permeability and %Fe has been highlighted as the largest permeability (353) is present at 27.15% Fe, while the lowest value (4) is present at 35.36% Fe, for 16 segment structures at 100MHz. It has been reported [100] that NiFe films with greater Fe composition produce harder magnetic properties, and that films with $Ni_{79}Fe_{21}$ produce the optimum permeability values. This correlation is important for the design of the inductor core as the permeability directly influences the inductance value.

The implications of the highlighted correlations between %Fe, resistivity, skin depth and permeability on the microinductors presented in chapter 3, must be considered when designing the core for optimal device performance. In this case, the skin depth is not considered as the thickness of the core is only 5μm and the inductor is tested up to a 10MHz. Hence, the skin effect is not present at this frequency and core thickness. However, the relationship between resistivity and permeability of the core has been highlighted, as lower %Fe leads to a higher permeability and resistivity. This effect is partly responsible for the relationship between the measured inductance value and Q-factor.

5.4.2 Mechanical properties

Figure 5.11 presents the wafer map of strain indicator structures, with expansion arm offsets of 6μm from the same wafers as wafer maps presented in figure 5.7, 5.8, 5.9. As has been reported in [136], the deflection of strain indicator structure is dependent upon composition (%Fe), and has been confirmed by correlation coefficient of 0.86.

This correlation between strain indicator structure rotation and %Fe composition has been reported in [136]. However, Schiavone [37] determined that Young's modulus increased with %Ni composition, and hence determined that as %Fe decreased stress increased. It is thought that the stiffness of the expansion arms is reduced as a result of lower Young's modulus values, which hence allows for greater rotation of the strain indicator structure.

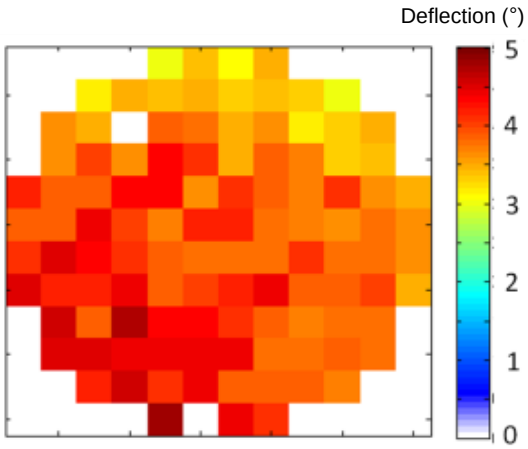


Figure 5.11: Wafer map of strain indicator deflection.

5.5 Conclusions

This chapter has reported a test chip that can be measured using automated optical and electrical measurement and thereby wafer map parameters and perform correlation analysis on electroplated ferromagnetic films. For the first time the permeability of the magnetic film has been quantified on wafer, using technology that is compatible with standard wafer electrical characterisation equipment. The ability to perform this measurement with relatively simple electrical measurements provides an opportunity for fast feedback on the magnetic performance of Permalloy depositions, which is a capability required for process control and verification measurements. The advantage of the approached described in this chapter is that it measures the magnetic properties of the skin depth and enables the magnetic uniformity over the wafer to be determined by spatially extracting the permeability at the frequency of interest. Its use of an RF electrical measurement means there is no need for any external electromagnet to produce a magnetic field. Additionally, the wafer does not require dicing.

448 RF and DC measurements of electrical resistance have been made across the wafer on the permeability test structures, presented in figure 5.3 (a). Using these measurements and corresponding thickness measurements, it has been possible to produce wafer maps of DC and RF electrical resistance, resistivity, skin depth and relative permeability.

Properties of an inductors NiFe core, such as its permeability and electrical resistivity are known to directly impact the inductance value and core eddy current losses, respectively. Using measurements extracted from the test chip, high correlation

coefficients (~0.9) between these properties and NiFe (%Fe) composition have been calculated.

It has been highlighted that electrical resistivity increases with %Fe and has a correlation coefficient of 0.91 for 8-turn structures. In contrast, it has been determined that relative permeability will decrease with %Fe and has correlation coefficients of -0.78, -0.87 and -0.92 for 8 turn permeability test structures measured at 15MHz, 20MHz and 100MHz, respectively. Hence, when designing an inductors core using NiFe compositions with high %Fe would be desirable to reduce core eddy current losses, and improve Q-factor. However, to improve inductance values, it would be desirable to used NiFe cores with lower %Fe composition. It is postulated that the permeability will reach its maximum at 20% Fe as described in chapter 2 and reported by Arnold [201]. This relationship between resistivity permeability and %Fe composition is partly responsible for the trade-off relationship between the inductors inductance value and Q-factor.

The limitation of this technique when measuring permeability is that for the skin depth model to be valid the thickness of the test structure must be greater than twice the skin depth value. Hence, as skin depth is inversely proportional to frequency, this technique becomes more effective as frequency is increased. A correlation between skin depth and %Fe has been highlighted. Hence, for %Fe compositions lower than those measured in this study, the effectiveness of this technique is improved, as it would be possible to measure permeability at frequencies below 15MHz for the same thickness of test structures.

Future work should include characterisation of NiFe films with a range of compositions, which includes 20%Fe. Additionally, there is an opportunity to determine the optimal compromise between magnetic, electric and mechanical properties required for the particular device application.

Chapter 6
Effect of Seed Layer on the Performance of Planar Spiral Microinductors

6.1 Introduction

Microinductors fabricated using MEMS based processes have been widely reported in the literature [15, 17, 26, 28-30, 77-80, 84, 87, 149, 202]. These processes typically involve a number of electro-deposition steps that require conductive 'seed' layers. It has been postulated that the use of magnetic seed layers, within the magnetic core, should improve electrical performance. However, detailed systematic experimental studies on any such improvement have not been documented in the literature. This chapter quantifies the advantages of implementing magnetic seed layers for the electro-deposition of magnetic cores.

Spiral microinductors have been fabricated using electrodeposition for both the coils and magnetic cores using conventional copper seed layers. Due to the low electrical resistivity (ρ=1.67$\mu\Omega$·cm) and paramagnetic behaviour (permeability, μ_r=1) of copper, these seed layers contribute towards higher eddy current losses without enhancing the inductance, while also acting as a thin 'screening layer'. This screening effect results from the eddy current formation in the seed layer, which creates an opposing magnetic field. Hence resulting in lower inductance and Q-factor values than would otherwise be the case with magnetic seed layers, and provides the motivation to quantitatively investigate the benefits of electroplating thick magnetic cores on ferromagnetic seed layers, such as nickel.

This work combines the characterisation of static magnetic properties and spatial variation measurements of compositional, electrical and mechanical strain, for NiFe films electroplated on both copper and nickel seed layers. While eddy currents in a conductive core cannot be eliminated completely, interrupting the electrical pathway through patterning the magnetic core can greatly reduce these parasitic currents. This work also reports the quantitative evaluation of planar spiral inductors with patterned magnetic cores. It examines the performance contribution from a Ni seed layer, on patterned magnetic cores, using the test bed inductor fabrication process described in

chapter 3, and is believed to be the first study of the effect of seed layers on planar spiral microinductors.

6.2 Characterisation of Electroplated NiFe films

The first required step was to determine whether NiFe electroplated onto Cu seed layers was the same as that electroplated on Ni seed layers. Hence, NiFe films electroplated on copper and nickel seed layers have been characterised in term of their composition to confirm that any changes in inductor performance result from the seed layer metal, and not changes in the composition of the NiFe core. Additionally, the effect of seed layer on the mechanical strain and electrical resistivity has been characterised using automated wafer mapping. These measurements are an essential component in the evaluation of the effect of the seed layer on the performance of the inductor and the formation of eddy currents in the magnetic core.

Half the test chip batch described in chapter 5 was fabricated with a copper seed layer, and the other half with a nickel seed layer in order to evaluate the effect of seed layer on the compositional, mechanical and electrical properties of the magnetic core. As described in chapter 5, 112 electroplated NiFe test chips were fabricated on four-inch silicon substrates, with both Ti (30nm)-Cu (300nm) and Ti (30nm)-Ni (300nm) seed layers, to a target thickness of 17µm. Automated wafer mapping was then employed to characterise the film composition and electrical resistivity at 448 points, and mechanical strain at 112 points, across the wafer. The effect of seed layer on the static magnetic properties of blanket NiFe layers was then determined using a BH-loop meter.

6.2.1 Compositional Characterisation

To characterise the composition of the electroplated NiFe on both copper and nickel seed layers, automated X-ray fluorescence (XRF) spectrometry measurements were carried out at the 448 points across each four-inch wafer to determine local values of %Fe composition. Wafer mapping was used to confirm the spatial variation of NiFe composition plated on the two seed layers, and wafer maps are presented in Figure 6.1. The variation in Fe content across the wafer has been deliberately created by the bath setup and agitation (as discussed in chapter 5) and the average composition for these

wafers was 30.09% and 30.45% Fe for films electroplated on copper and nickel seed layers, respectively.

As the target composition for the magnetic core was $Ni_{80}Fe_{20}$, the characterisation of NiFe composition was also undertaken for films closer to 20% Fe composition, using XRF. These films electroplated on copper and nickel seed layers produced average %Fe compositions of 20.11% and 19.86%, respectively.

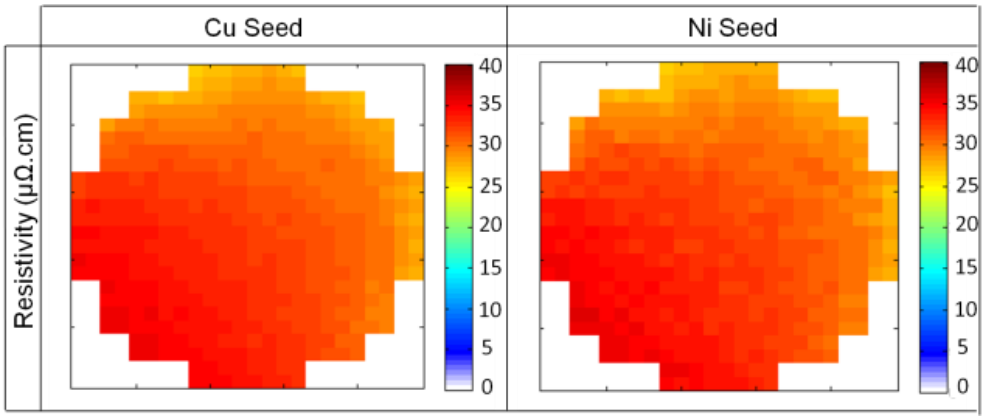


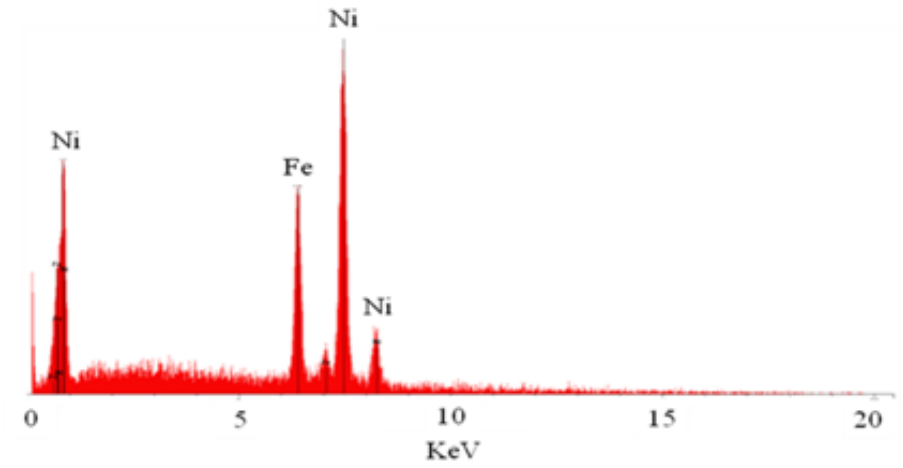
Figure 6.1: *Composition wafer maps, for NiFe films electroplated on both Ni and Cu seed layers.*

In addition to XRF, energy dispersive X-ray (EDX) spectroscopy was also used to confirm that there was a similar composition on films plated on both seed layers. These EDX spectra are presented in figure 6.2, and show similar peak width and heights for both films.

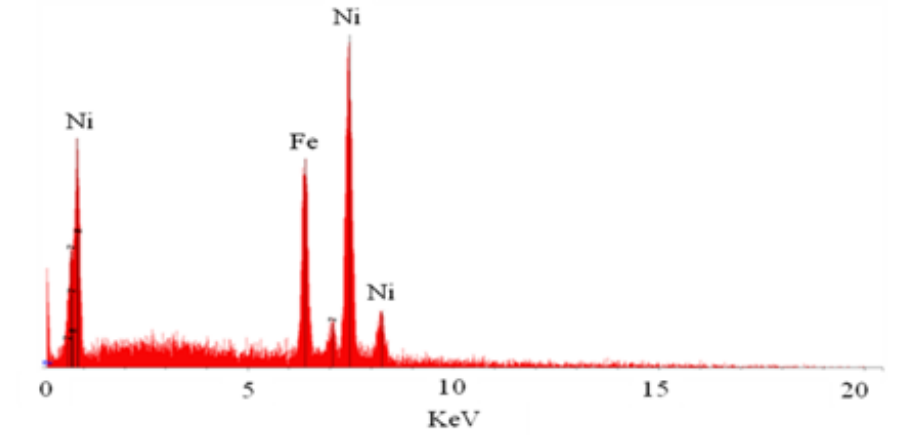
Composition wafer maps and EDX spectra indicate minimal differences in the composition, which suggests the seed layer has little or no effect on the composition of the electroplated NiFe. Hence, any change in inductor performance is not the result of compositional changes of the electroplated core.

6.2.2 Characterisation of Mechanical and Electrical Properties

The effect of seed layer on the mechanical and electrical properties of electroplated NiFe films has been characterised using the permeability and strain indicator test structures presented in chapter 5 (see figure 5.2 (a), (c) and (d)). The resulting electrical resistivity and mechanical strain were characterised using the same testing setup and methodology described in chapter 5.



(a)



(b)

Figure 6.2: *EDX spectra for NiFe electroplated on (a) copper and (b) nickel seed layers.*

Wafer maps of NiFe strain and resistivity are presented in figure 6.3. The average rotation and resistivity for these structures was 3.2˚, and 21.47μΩ.cm for films electroplated on copper, and 3.9˚ and 23.53 μΩ.cm for NiFe electroplated on nickel seed layers. The average strain was measured to be 18% lower for NiFe films electroplated on copper seed layers, and it is thought that this seed layer may provide some stress relief for the NiFe film. However, it is unclear whether this is the result of stress reduction in the NiFe film, or a reduction in the deflection of the strain indicator structure due to lower tensile stress in sputtered copper compared to nickel [203, 204].

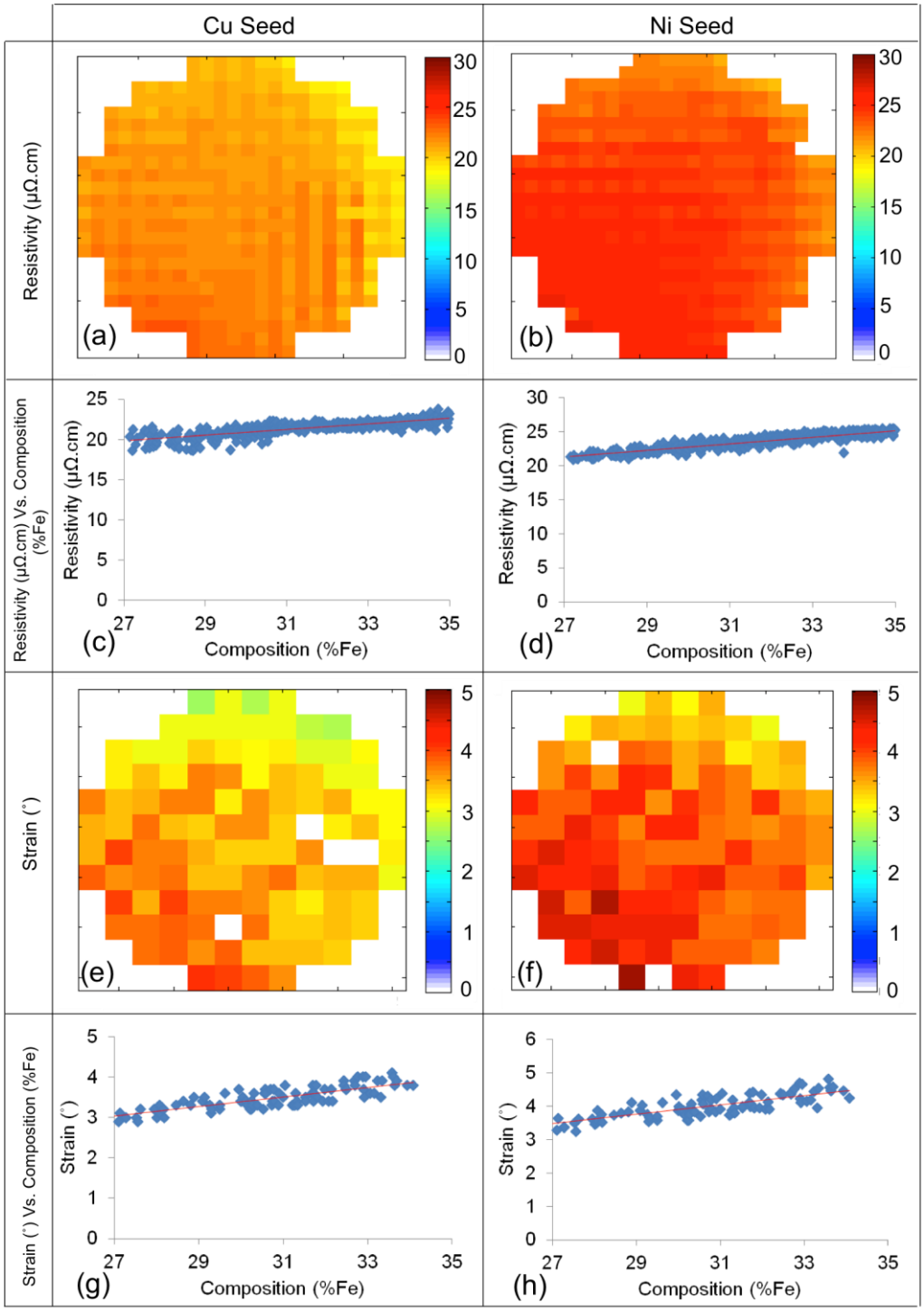


Figure 6.3: *Wafer maps of electrical resistivity ((a) and (b)), and plots of electrical resistivity vs. %Fe composition ((c) and (d)), electroplated on Cu and Ni seed layers, respectively. Additionally, wafer maps of mechanical strain ((e) and (f)), and plots of strain vs. %Fe composition ((g) and (h)), electroplated on Cu and Ni seed layers, respectively.*

The 9.6% increase in resistivity when nickel replaces a copper seed layer for electroplating NiFe is simply due to the higher resistivity of the nickel seed layer (ρ=6.99$\mu\Omega$·cm) and is beneficial as it reduces the magnitude of eddy currents in the inductor's NiFe core. The value of resistivity of NiFe has been reported previously to be 20$\mu\Omega$.cm [205] and 17-23$\mu\Omega$.cm [206] for $Ni_{65}Fe_{35}$, and these values are in good agreement with the values measured in this chapter.

Figure 6.3 also presents resistivity and strain measurements as a function of the NiFe composition for each corresponding point on the wafer. As has been reported in [136] strain increases with increasing percentages of %Fe composition. The correlation coefficient for strain with respect to composition has been determined as 0.85 and 0.86 for films electroplated on copper and nickel respectively. As was discussed in chapter 5, the film resistivity also increases with composition and has correlation coefficients of 0.82 and 0.91 for films electroplated on copper and nickel, respectively.

6.2.3 Characterisation of Magnetic Properties

Hysteresis BH-loop measurements were performed on unpatterned 4µm thick $Ni_{75}Fe_{25}$ films, electroplated on Ni and Cu seed layers, and are presented in figure 6.4. BH-loops were measured using the same dedicated Shb Instruments equipment comprising of a 10Hz oscillating electromagnet and pickup coils, as was used in chapter 5. These films present similar coercive field of 0.04A.m and 0.036A.m for films with nickel and copper seed layers respectively. However, at saturation magnetisation the magnetic flux density in the films electroplated on Ni seed layer is 2.3% greater than that of copper seed layer. This is attributed to the approximate 7.5% increase in the volume fraction of magnetic material in the sample, which has been reported to be proportional to flux density at saturation magnetisation [75].

6.3 Characterisation of the fabricated Microinductors

Building upon the work characterising the effect of seed layer on the electrical, magnetic and compositional properties of electroplated NiFe; planar spiral microinductors have been fabricated to characterise the effect of seed layer on the

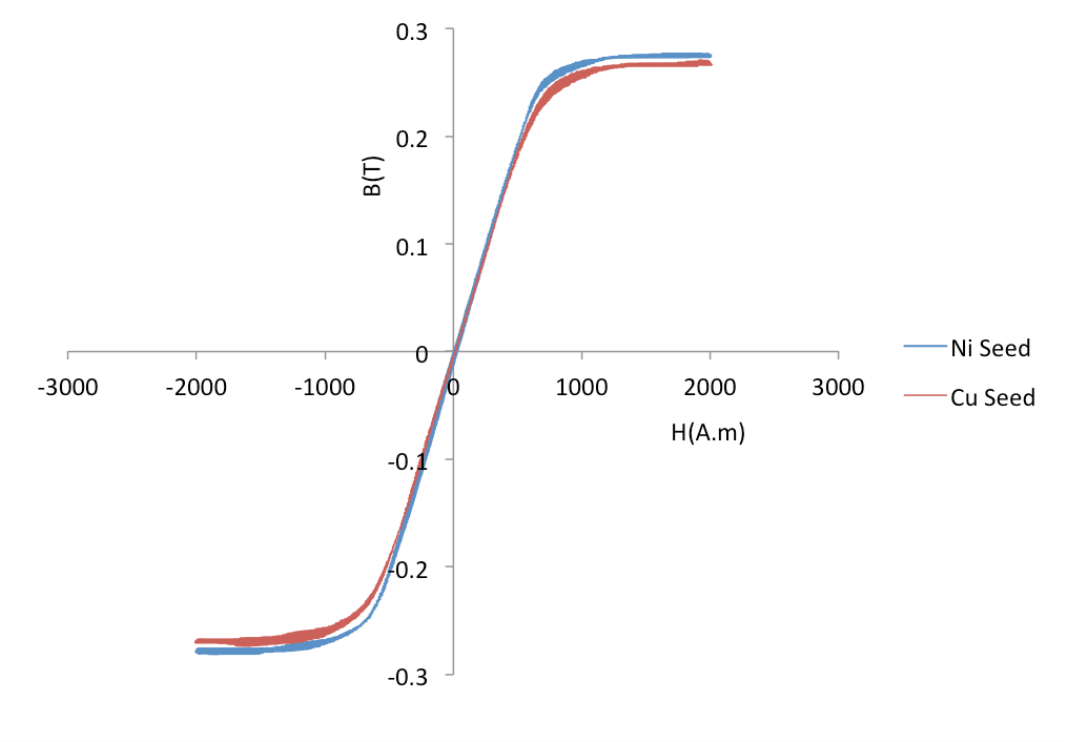


Figure 6.4: *Hysteresis (BH-loop) measured for a 4μm thick NiFe film electroplated on Ni and Cu seed layers.*

performance of these inductors. The completed inductor architectures were fabricated using the test bed inductor process described in chapter 3. As was the case when characterising the properties of the electroplated NiFe on each seed layer, half of the batch was fabricated using Ti(30nm)-Ni(300nm) seed layers, and the other half using conventional Ti(30nm)-Cu(300nm), for electroplating of both NiFe layers.

The fabricated inductors have the same architectures as those presented in figure 3.10 (b-d), where the NiFe encapsulates 52% (type 1), 82% (type 2), and 99.5% (type 3) of the inductors coil. The magnetic cores were fabricated with a number of different patterns presented in figure 6.5. Figure 6.6 shows cross-sections of the inductors, with unpatterned magnetic (with and without an air gap) and mesa structures. These cross-sections were obtained by dicing, which was followed by polishing of the cross-section, and then photographed using optical microscopy. The cross-sections confirm the gaps between copper coils have been completely filled with Parylene and NiFe is "wrapped around" the copper coils, with a small air gap between the top and bottom NiFe layers.

As in chapter 3, the inductors were measured in the 200kHz to 10MHz frequency range using a HP4275A LCR meter. The DC resistance measured for all coils was 1.86 ± 0.04 Ω. Hence, any change in Q-factor is not the result of differences in coil resistance, but is due to the effect of the different seed layer metals. Figure 6.7 presents the inductance and Q-factor spectra for the type 1 architecture with a Ni seed layer, and compares the performance of devices with the magnetic material patterns as shown in figure 6.5. Figure 6.8 compares the inductance achieved for each core pattern with inductor architecture, to highlight the relationship between volume fraction of NiFe and measured inductance for coils with a Ni seed layer at 10MHz. Figure 6.9 compares the inductance and Q-factor spectra for the different magnetic film patterns for both copper and nickel seed layers.

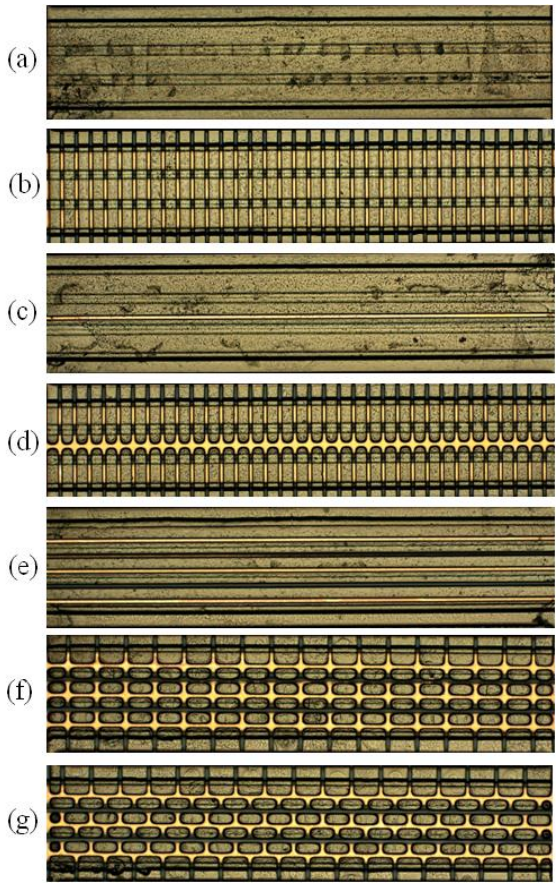


Figure 6.5: *Patterned NiFe core structures; (a) unpatterned; (b) bar structures perpendicular to the coil; (c) unpatterned with a 10µm air-gap; (d) bar structures perpendicular to the coil with a 10 µm air-gap; (e) bar structures parallel to coil; (f) mesa structures without offset; (g) mesa structures with offset.*

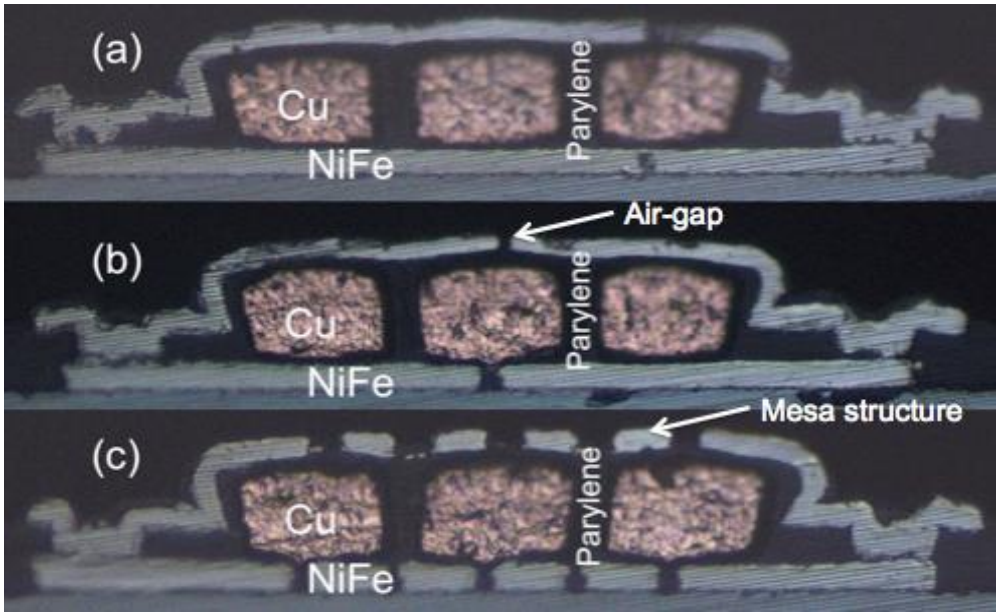
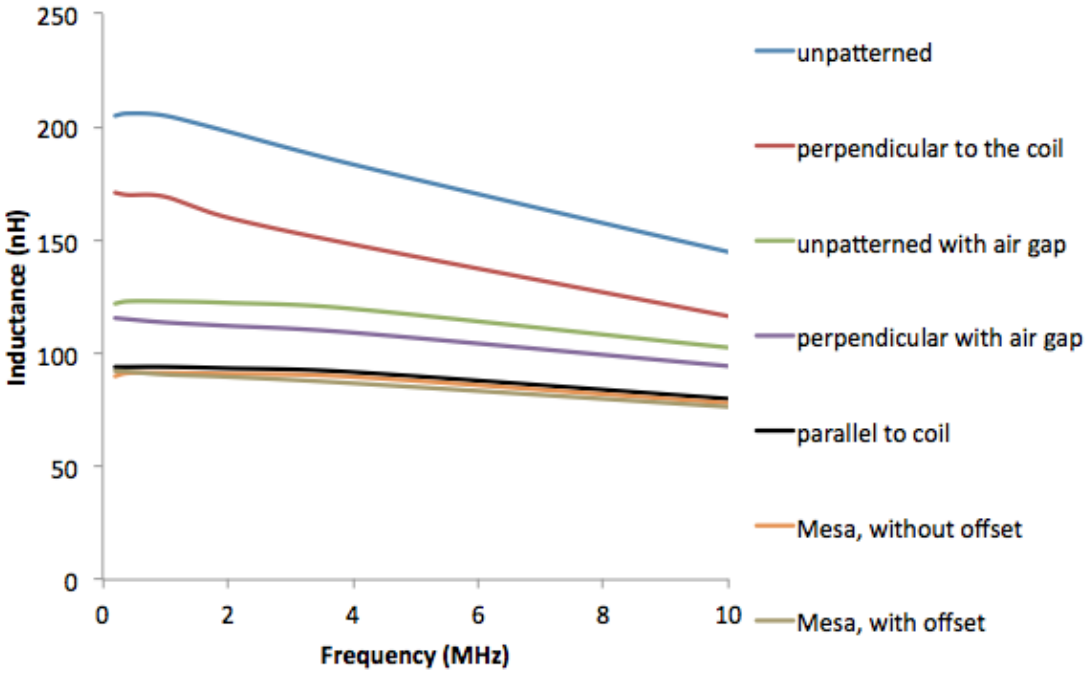
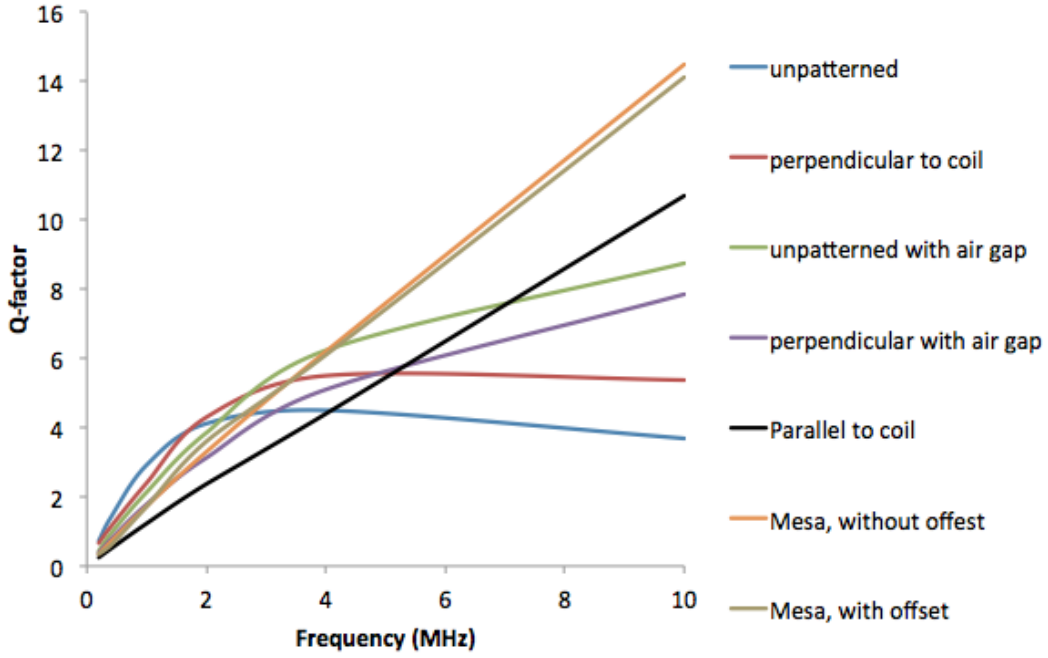


Figure 6.6: *Cross-section of (a) unpatterned, (b) core with air gap and (c) mesa structure inductor.*



(a)

Figure 6.7: *Inductance (a) spectra of type 1 inductors with Ni seed layers and patterned magnetic core.*



(b)

Figure 6.7: *Q-factor (b) spectra of type 1 inductors with Ni seed layers and patterned magnetic core.*

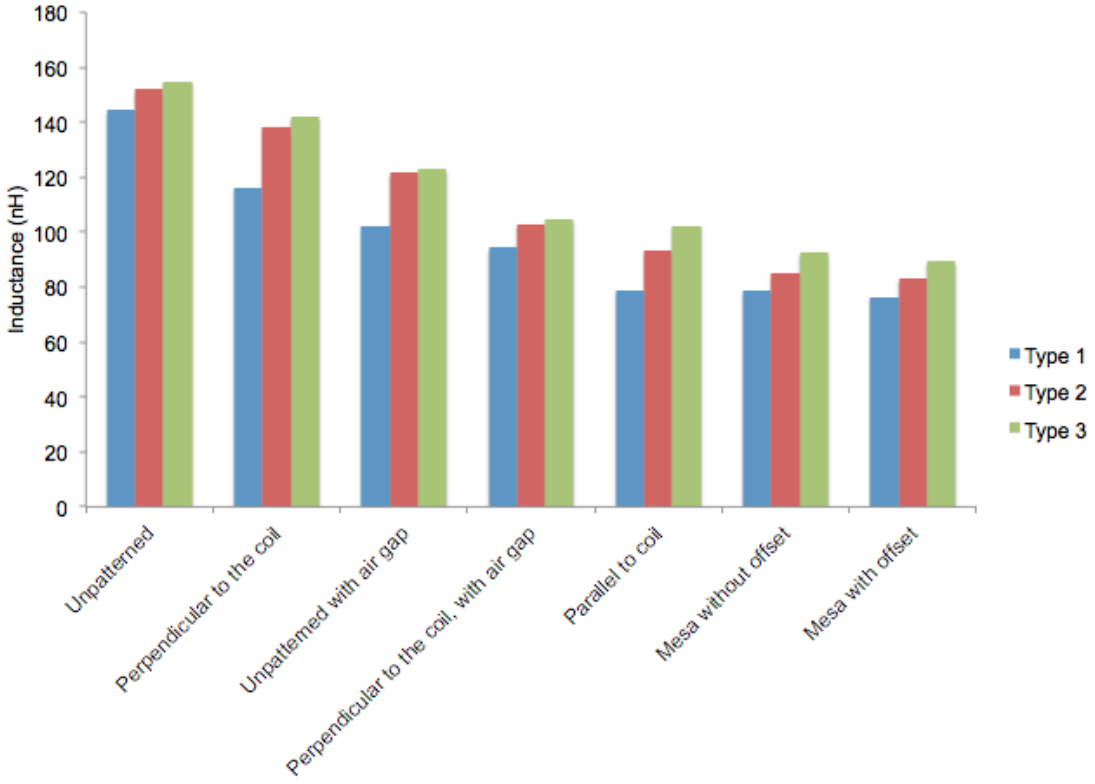


Figure 6.8: *Inductance achieved for each architecture and patterned core with Ni seed layer at 10MHz.*

As was discussed in chapter 3, it is well understood that there is a correlation between the volume fraction of NiFe, in the inductors core and measured inductance value. Hence, from figure 6.7, as would be expected; coils with unpatterned NiFe (which have the largest volume fraction of magnetic material) produce the largest inductance value (144nH, at 10MHz). However, as the core is unpatterned, eddy currents flow through the entire core, resulting in higher losses and hence result in the lowest measured Q-factor for the type 1 architectures (3.7 at 10MHz). Figure 6.8, further highlights the relationship between volume fraction of magnetic material and achieved inductance value, by plotting inductance (at 10MHz) for each core pattern and comparing all three levels of NiFe encapsulation of the coil. Type 3 inductors (99.5% encapsulation) consistently achieve the largest inductance value for each patterned core. Clearly, as NiFe volume fraction is increased so too is the value of inductance.

Unpatterned magnetic cores have been incorporated into a number of inductors reported in literature [9, 17, 24, 28, 30, 31, 82, 84, 86, 202]. Meere [82] has achieved inductances between 20nH to 200nH for planar spiral inductors with $Ni_{45}Fe_{55}$ cores wrapped around the inductor's coils. These components had 2 to 5 turns and footprint of 0.5 mm^2 to 2.5mm^2, respectively. While it is known that the relative permeability of $Ni_{80}Fe_{20}$ is greater than that of $Ni_{45}Fe_{55}$ [81, 201], this latter composition has been used as it has been shown to extend the operational frequency to 20MHz [28].

From figure 6.7 and 6.9, the introduction of an air-gap into unpatterned cores and cores with bar structures perpendicular to the coil reduce the inductance value by 29.4% and 18.9%, respectively. At the same time measurements of Q-factor, increase by 71% and 55%, respectively, for inductors with the type 1 architecture and Ni seed layers at 10MHz. The function of the air-gap is to modify the shape of the BH-loop, such that relative permeability is reduced and the saturation magnetisation is increased. The addition of the air-gap also introduces losses as a result of the fringing flux phenomenon, whereby the flux lines in the air-gap expand to occupy space outside of the magnetic core's cross-section. This consequently results in a reduction in magnetic flux density and hence relative permeability. Furthermore, the dimension of the air gap clearly affects the level of fringing [207-209]. Therefore, a

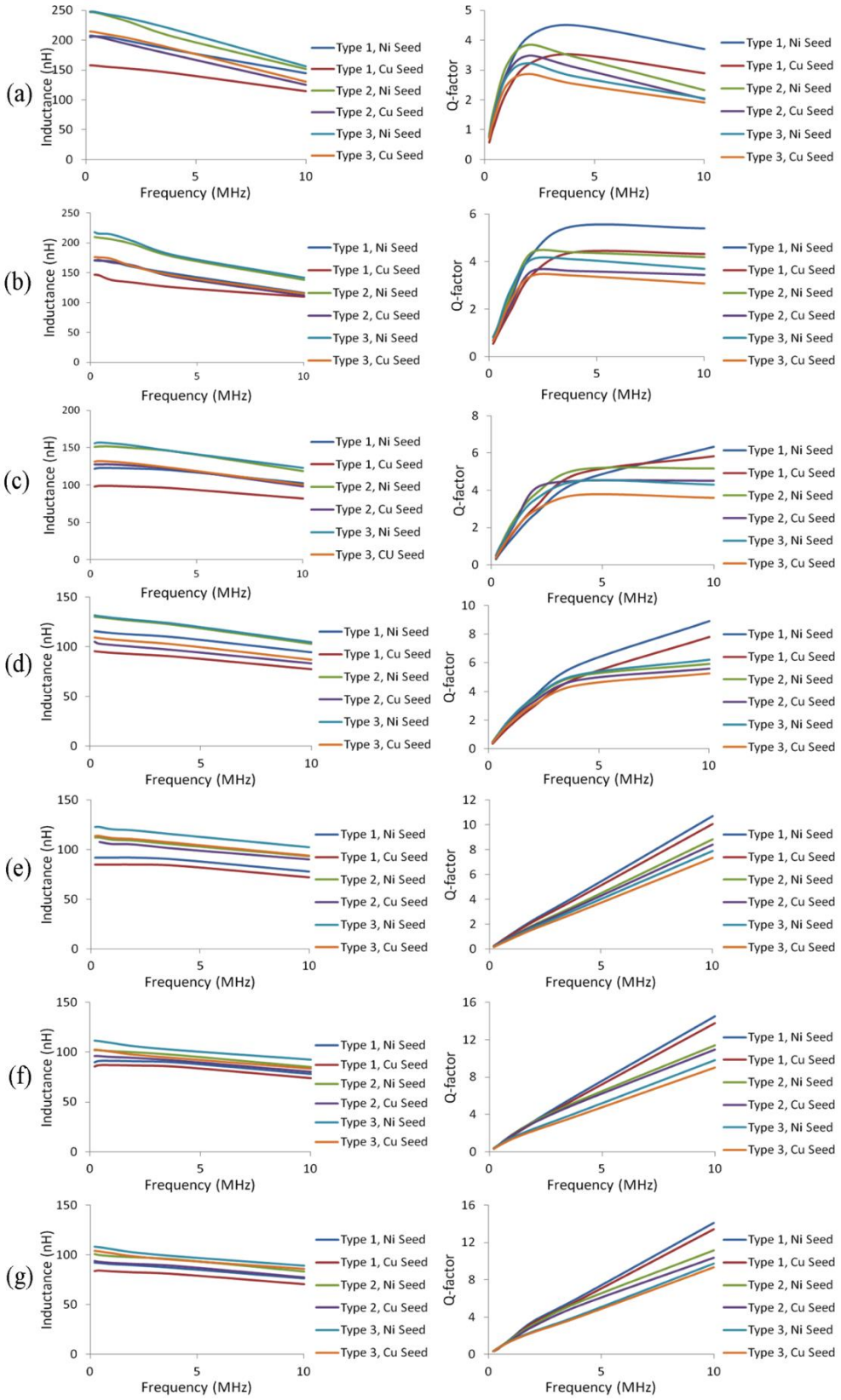


Figure 6.9: *Q-factor and inductance spectra for (a) unpatterned; (b) bar structures perpendicular to the coil; (c) unpatterned with a 10 µm magnetic gap; (d) bar structures perpendicular to the coil, with a 10 µm magnetic gap; (e) bar structures parallel to coil; (f) mesa structures without offset; (g) mesa structures with offset.*

reduction in inductance with the inclusion of an air-gap is to be expected. However, an air-gap in the core is often incorporated into the structure in order to increase the inductor's saturation current [16, 210].The effect of a 20μm air gap on three-turn spiral inductors with unpatterned $Ni_{45}Fe_{55}$ cores has been reported in [211]. The core of these inductors had been electroplated to include magnetic anisotropy, with the hard axis perpendicular to the coils. The effect of the air-gap results in a 17% to 23% reduction in inductance and an 8.33% to 12% increase in Q-factor, at 10MHz, for the inductor architectures reported in this work. The type 1 unpatterned core inductors, and those with air-gaps reported on in this chapter (figure 6.7 and 6.9), indicates that the air-gap has a greater effect on inductance and Q-factor than those reported by Wang [26]. The differences observed are probably related to the single 20μm air gap used in [85] having a larger fringing field and therefore higher flux fringing losses. Additionally, the two 10μm air gaps located both under and on top of the coils fabricated in this work also more effectively reduced eddy currents.

Inductors with bar structures parallel to the coils have not been reported in literature. However, this pattern can be considered as a continuous film with three air gaps on both top and bottom NiFe layers. Hence, the 45% reduction in inductance and 189% increase in Q-factor (at 10MHz), for type 1 inductor with Ni seed layers, is attributed to flux fringing phenomenon and reduction of eddy currents, compared to inductors with unpatterned cores. It is clear from figures 6.7 and 6.9 that as the frequency increases; the Q-factor reduces at a greater rate for inductors with unpatterned cores without air-gaps, than those with air-gaps. This would suggest that the introduction of the air-gap also increases the inductor's operational frequency.

Inductors incorporating mesa structures, which have the lowest volume fraction of NiFe, produce the smallest inductance (78nH) and largest Q-factor (14.5) at 10MHz. The low inductance value with this architecture is clearly the result of the low volume fraction of NiFe, and fringing flux losses between mesa structures. In contrast, this high Q-factor is probably due to lower eddy current formation resulting from the reduced current paths associated with the mesa structures. The increasing Q-factor observed with frequency for the mesa pattern has previously been reported in [16], with Q-factors still rising at 1GHz.

It is clear from figure 6.9 that the use of a Ni seed layer has improved the inductance and Q-factor by 26% and 19% respectively at 10 MHz for unpatterned inductors. It is also clear that improvement is dependent upon the structure of the magnetic core. Inductors with mesa structures, without an offset, produced the smallest increase in inductance and Q-factor (5.2% and 4.9% respectively) for type 1 inductors, at 10 MHz. It should also be noted that for all Q-factor and inductance spectra, presented in figure 6.9, the inductors that incorporate a Ni seed consistently produce higher Q-factors and inductance values, than their counterparts with Cu seeds.

Again, figures 6.8 and 6.9 also show the effect of NiFe volume fraction on the performance of these inductors. As would be expected, inductors with the highest NiFe volume fraction (Type 3, unpatterned, with Ni seed) produce the highest inductance value (155 nH at 10MHz) and the lowest Q-factor (2.05). These inductors also show the greatest enhancement of inductance from the air-core value (41nH). Inductors that use Permalloy mesa structures produced the lowest inductance value (78.07nH, type 1 with Ni seed) and the highest Q-factor (14.5), at 10MHz.

6.4 Inductor Benchmarking

Figure 6.10 presents the relationship between inductance (at 10MHz) and the number of turns for devices reported in literature, and compares them with the type 1 inductors fabricated in this work. It clearly demonstrates the requirement to increase the number of turns to achieve higher inductance values. In contrast figure 6.11 presents a similar comparison between Q-factor and inductance density, at 10MHz. These figures have been reported in chapter 2. However, this chapter compares inductors reported in literature with inductors developed in this thesis.

An important achievement is the clear improvement in both Q-factor and inductance density for each inductor when fabricated with Ni seed layers, and this is clearly presented in figure 6.11. As was already mentioned in this chapter, this is the result of the increased volume fraction of magnetic material; greater resistivity of Ni than Cu and a reduction in the shielding effect from the seed layer. The impact of this improvement will allow for the fabrication of inductors with greater efficiency and lower device footprints, thus allowing for more compact power supply solutions.

Inductors reported in this chapter are competitive with those reported by Wang [85] with inductance values of 140nH and 130nH, at 10MHz, similar to those reported in this chapter. In addition these inductors deliver a similar air core inductance (38nH), and hence a similar enhancement in inductance as a result of the magnetic core, for unpatterned magnetic cores with Ni seed layers. However, in addition to uniaxial anisotropy induced in the core during electroplating, the architectures reported by Wang [85] also incorporate two NiFe layers on the bottom core. From figure 6.11, the inductance density of these inductors is lower than that of those reported in this chapter, as a result of a greater device footprint (5.69mm^2). Additionally, the magnetic core appears to encapsulate only 80% (approximated from image of the inductor) of the coils. Hence when comparing with type 2 inductors (unpatterned with Ni seed layers) which have similar level of NiFe encapsulation (82%), inductance is not surprisingly 8% and 14% lower than those reported in this chapter. From figure 6.11, inductors developed by Wang [85], produce a greater Q-factor (2.4 and 2.8) than the type 2 inductors. This is to be expected given the relationships between increasing %Fe and resistivity and decreasing permeability discussed in chapter 5. Hence, when comparing inductors with different cores (e.g. $Ni_{45}Fe_{55}$ with $Ni_{80}Fe_{20}$) those that have the same number of turns and similar levels of NiFe encapsulation should produce inductance values in the ratio of their permeability. The Q-factors of the inductors reported by Wang [85] are expected to be greater, as a result of higher core resistivity.

It is interesting to note that the inductors reported by Wang [26] present a similar Q-factor (2.4 to 2.8) to the unpatterned type 1 inductors. Considering the large surface area of the core reported in [26, 29], this could be the source of large eddy current losses. Additionally, the type 1 architecture, reported in this chapter splits the core into 4 segments, compared to the 2 segments reported in [26], hence constraining eddy currents.

From figure 6.10, Wang [86] also reported 3 turn inductors with $Ni_{80}Fe_{20}$ cores including Cr laminations and their measured inductance was 0.9nH, and 0.33nH (air core), an inductance enhancement of 172%. The low inductance measured for the

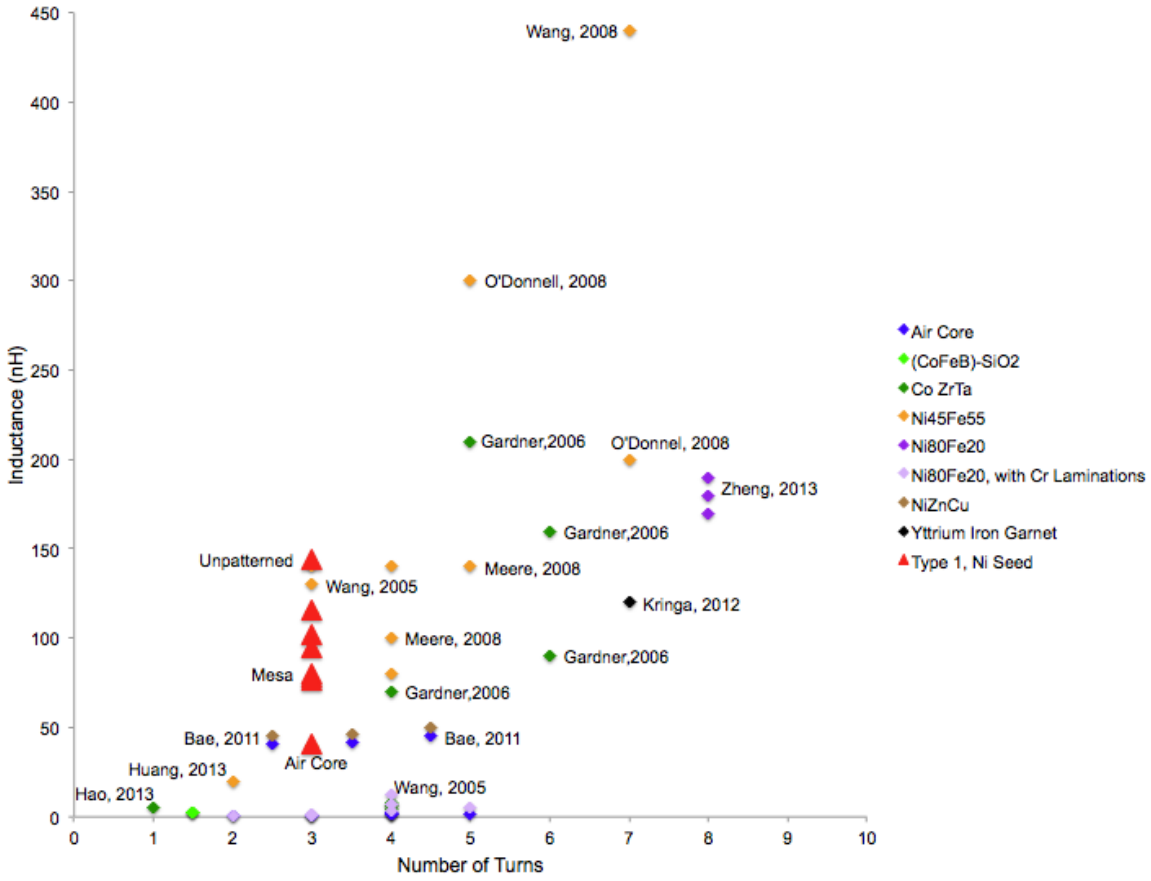


Figure 6.10: *Comparison of type 1 inductors, with Ni seed layers to inductors reported in literature (inductance value, at 10MHz, with number of turns) [9, 17, 28-30, 77-80, 84, 87, 150]. The large symbols are results from this work.*

inductors developed by Wang, is the result of a small device footprint of 0.0016mm^2. In contrast, this inductor exhibits the largest inductance density of 562.5nH/mm^2 reported in literature.

Yang [87] reported 8 turn $Ni_{80}Fe_{20}$ core inductors, with inductance values of 170nH to 190nH and inductance densities from 4.17nH/mm^2 to 4.95nH/mm^2. The low inductance densities, compared to others reported in this chapter results from the architecture only using NiFe below and in the centre of the inductor coils.

While the purpose of the work presented in this thesis has not been the optimisation of the developed inductors, it is clear from figures 6.10 and 6.11 that a number of improvements can be implemented to improve both the inductance and Q-factor. As

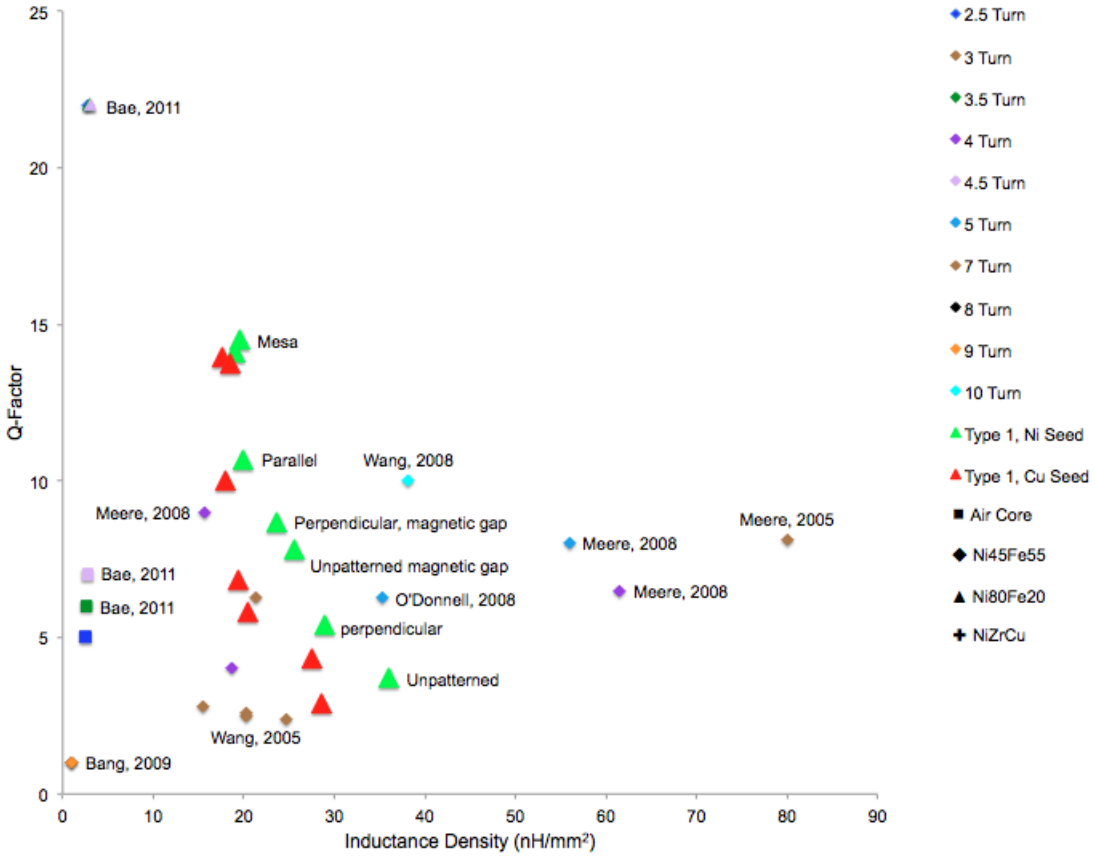


Figure 6.11: *Comparison of type 1 inductors to inductors reported in literature (inductance density with Q-factor, at 10MHz) [9, 28, 30, 77-80, 82, 84, 86, 87, 211]. The large symbols are results from this work.*

figure 6.10 has highlighted the relationship between inductance and number of turns, clearly utilising the entire area occupied by the device would improve inductance density. Using the modified Wheeler equation reported in [43] the air-core value of the current three-turn inductor coil has been calculated to be 38.6nH, which is in good agreement with the measured inductance of 41nH. While maintaining the same coil geometry, it is clear that the device footprint could be utilised for inductors with up to 15 turns, resulting in an increase in air-core inductance of up to 229nH. Assuming the enhancement as a result of the magnetic core is the same as for the three-turn inductors presented in this work, it is estimated that the inductance value of type 1 inductors with Ni seed layers would improve up to 803.79nH, at 10MHz. However, this estimate does not take into account additional losses as a result of larger volume fraction of magnetic material.

Reducing the gap between the coils from 10μm to 5μm only improved the calculated air-core inductance by 0.7nH, for the three-turn inductor reported in this chapter. Hence, reduction of the gap between the copper coils should not be considered for the optimisation of this inductor.

As was discussed in chapter 2, Glickman [48] produced the largest initial permeability value for Permalloy reported in literature (8500), by incorporating uniform agitation across the wafer surface during electroplating. Furthermore, Glickman [48] noted further improvement in permeability as a result of low contamination from iron oxide in the electroplated Permalloy film. This was achieved by maintaining the electroplating bath in an inert nitrogen environment. If a similar initial permeability could be achieved to Glickman [48], and assuming that permeability decayed at the same rate with frequency as the NiFe films reported in this chapter, it is estimated that the inductance could be improved to 1.1μH, for type one inductors with Ni seed layer at 10MHz.

From figure 6.10, the largest inductance per turn (50nH) was reported by Gardner [17], using CoZrTa core. However, using this core material would only increase the inductance value by 6nH for the type 1 inductors at 10MHz. Hence, the greatest improvements in inductance are likely the result of utilising the full inductor footprint with coils and optimising the NiFe electroplating bath setup. Therefore, the estimated maximum inductance that can be achieved using both of these strategies on

the inductors designs/technology reported in this thesis is 6.3μH. Figure 6.13 presents the estimated improvements for type 1 inductors with different patterned magnetic cores used in this work.

While there is clear value to increasing the number of turns and optimising the bath setup, it should be noted that these improvements are based upon theoretical multipliers and the fully optimised result takes no account of any interactive effects that may result when multiple parameter modifications are involved.

Bae [84] achieved the greatest Q-factor reported in literature by using a non-conductive core. However, the draw back of this was that the core deposition process required sintering at 800°C, and hence this process could not be incorporated into a

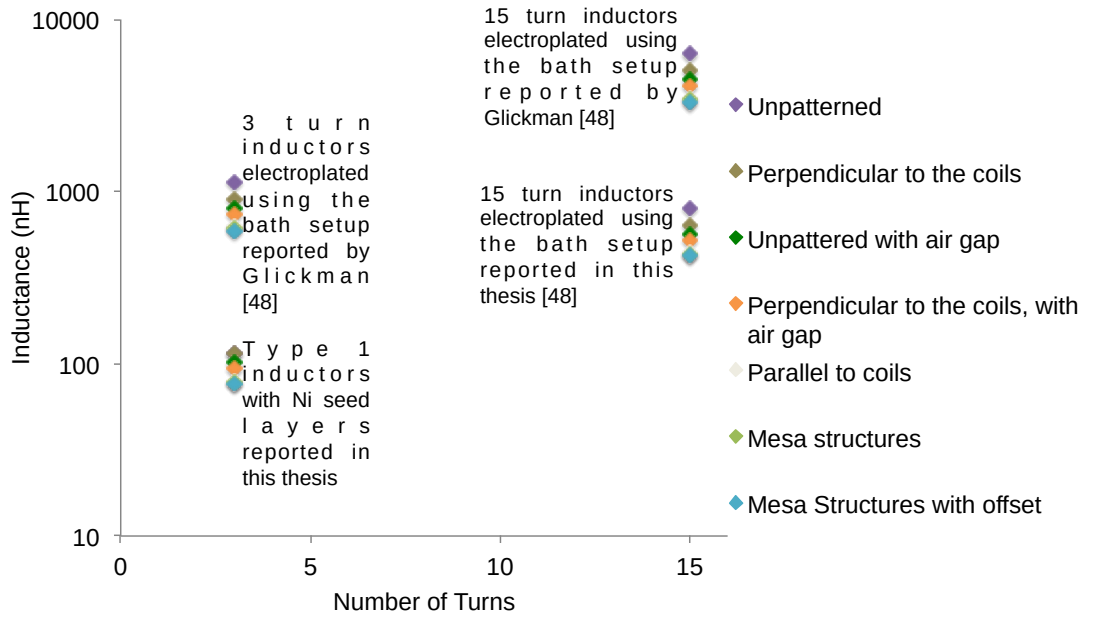


Figure 6.12: *Comparison of type 1 inductors, with Ni seed layers to estimates of optimised inductors in terms of increasing number of turns and using electroplating bath setup developed by Glickman [48].*

MEMS inductor fabrication process, with a future aim of integrating with silicon IC. However, this paper does highlight the importance of reducing eddy currents in the magnetic core to improve efficiency.

One possible option to mitigate eddy current losses in the NiFe core, while improving inductance density could be a further improvement in inductors with mesa structure patterned cores. By aggressively reducing the gap between the structures, and the size of the mesa structures close to that of a single magnetic domain to maximise the volume fraction of magnetic material, whilst minimising eddy current losses. It is well known that the behaviour of magnetic materials patterned at dimensions close to single magnetic domains would behave markedly different compared to continuous films, as the shape of the pattern and interaction between adjacent mesa structures defines the behaviour of the patterned core. Hence, it is postulated that this method could further improve performance by inducing uniaxial shape anisotropy in the core. This possible approach will be discussed further in chapter 7.

6.5 Conclusions

This chapter has detailed the first evaluation of the contribution of seed layers to the performance of planar inductors, which employ a NiFe core both above and below the copper coil.

The effect of seed layer on composition, electrical resistivity and mechanical stress has been studied by automated wafer mapping of test structures. This work has shown that seed layer has no effect on the composition of the electroplated NiFe. However, as expected electroplating on a nickel seed layer increases the electrical resistivity by 9.6%. This increase in resistivity reduces eddy currents in the inductor's NiFe core, while at the same time improving inductance value.

Measurements of strain indicator structures presented an 18% lower angular deflection for NiFe films electroplated on copper seed layers,. However, it is unclear whether this is the result of a stress reduction in the NiFe or result of a reduction in the deflection of the strain indicator structure, due to lower tensile stress in sputtered copper compared to nickel [203, 204].

The static BH-loop measurements performed on unpatterned 4µm thick $Ni_{75}Fe_{25}$ films and electroplated on Ni and Cu seed layers presented very similar coercive fields. However, at saturation magnetisation the magnetic flux density in the film electroplated on Ni seed layer is 2.3% greater than that of copper seed layer. This increase in saturation magnetisation has been attributed to an increase in the volume fraction of magnet material.

Using the test bed inductor process, presented in chapter 3, planar spiral microinductors have been fabricated to characterise the effect of seed layer on the performance of inductors with patterned magnetic cores. Inductance and Q-factor have been shown to range from 76.5nH to 155nH and 2.05 to 14.5 at 10MHz, respectively, depending upon how the NiFe core has been patterned and the degree of encapsulation of the coil in NiFe. The effect of each pattern on measured inductance and Q-factor has been discussed.

The replacement of the conventional copper seed layer with nickel seed layers has shown to improve both inductance and Q-factor by 5.2% to 26% and 4.9% to 19%, at 10 MHz for type 1 inductors. This improvement is clearly dependent upon how the

magnetic core has been patterned. The impact of this improvement will allow for the fabrication of inductors with greater efficiency and lower device footprints, thus allowing for more compact power supply solutions.

This chapter has also benchmarked inductors reported in this chapter against inductors reported in literature, in terms of the achieved inductance per number of turns and Q-factor against inductance density. It was found that the type 1 inductors with unpatterned magnetic cores and Ni seed layer are competitive with Wang [85] in that they present similar inductances values for the same number of turns and similar enhancement as a result of Q-factor. However, a number of strategies for the improvement of inductance with the developed inductors have been outlined. These include fully utilising the device footprint with coils and optimising the electroplating bath setup.

From this benchmarking work Bae [84] has highlighted the importance of mitigating eddy currents in the core to achieve high Q-factor inductors, by using non-conductive cores. The use of this core material is not feasible for integration with the inductor presented in this chapter. Hence, a strategy to aggressively reduce the size and spacing of the mesa structures has been outlined, which is expected to significantly reduce eddy current formation, while increasing the measured inductance.

Chapter 7
Conclusions and Future Work

7.1 Introduction

The focus of this thesis has been the characterisation of materials and processes to improve the performance and reliability of microinductors. This chapter summarises the most important achievements and conclusions in this thesis. Additionally, suggested future work will be presented.

7.2 Achievements and Main Conclusions

7.2.1 Development of test-bed inductor process with short turnaround time

As detailed in chapter 2, the patterned core inductor process developed by National Semiconductor has a turnaround time of one month. This long turnaround time is typical for microinductor fabrication. Hence, for evaluating the suitability of materials and processes a test-bed inductor fabrication process, with a short turn-around time of one week has been developed.

7.2.2 Integration of Parylene as a Structural and Dielectric Layer

SU-8 is a common choice for an inductor's structural and dielectric layer [15, 18-31]. However, as SU-8 suffers from issues with high residual stress and adhesion it was desirable to identify and characterise new materials and processes that could replace SU-8 in the microinductor fabrication process. Chapter 3 detailed the characterisation of Parylene and demonstrated that this material can be successfully used in the fabrication of planar spiral microinductors with thick electroplated copper coils and NiFe cores.

Using Scotch-tape testing, this study evaluated the good adhesion of Parylene to materials used in the test-bed inductor fabrication process.

Additionally, the Parylene fill performance was evaluated and confirmed that Parylene can completely fill 3:1 aspect ratio trenches. FIB cross-sections confirmed that the gap between high aspect ratio trenches was conformally coated with Parylene, without the formation of voids when Parylene was deposited onto trenches with positive sidewalls.

A void was clearly formed when Parylene was deposited onto trenches with negative sidewalls. However, as Parylene is deposited under vacuum (0.1Torr), and as no corrosive or solvent chemistry is involved in the deposition process, it is thought that this void would probably be relatively benign. Hence, this void should not affect the reliability of the fabricated device.

Parylene deposited on top of the copper coils has been successfully polished using a CMP process, with a removal rate of 833±33nm/min, and an average surface roughness after polishing of 7.9nm, between the 30μm thick copper tracks.

Building upon work evaluating and characterising Parylene processing, microinductors with electroplated NiFe cores have been successfully fabricated using the test-bed inductor process, to confirm the capability of Parylene as a structural and dialectic layer in this fabrication process.

A further advantage of using Parylene instead of SU-8 in the inductor fabrication process is that the maximum processing temperature is reduced from 200˚C (SU-8 hard baking process), to 140˚C (soft baking temperature of NR2-20000P). This is known to reduce the stress in the NiFe core [169, 170]. However, while the residual stress in Parylene films is expected to be low due to its room temperature deposition process, inductor fabrication requires thermal processing. Hence, it was necessary to characterise residual stress as a result of thermal treatment, and compare this with SU-8 under different processing conditions. Chapter 4 characterised the residual stress in SU-8 and Parylene films by combining independent measurements of strain indicator structures and local nanoindentation measurements to determine Young's modulus.

This study confirmed low tensile strength in Parylene films following deposition (5.52MPa). However, the residual stress increased to 14.07MPa and 30.05MPa following thermal treatment at 70˚C and 140˚C, respectively. When Parylene films were heated to 200˚C strain indicator structures fractured, indicating that the stress in the film is greater than the ultimate tensile strength of Parylene. Therefore, when considering the use of Parylene as a dielectric layer, thermal treatment must be carefully considered.

Additionally, it is important to note that Parylene annealed at 140°C develops a comparable level of stress with SU-8 3005 annealed at 150˚C or 200˚C followed by gradual cooling.

The impact of incorporating Parylene into the inductor fabrication process is the development of inductors with improved reliability, yield and shorter turn around times in comparison to those which incorporate SU-8. This is a result of the reduced processing steps, processing temperature, and better adhesion detailed in the development of the Parylene microinductor.

7.2.3 Correlation of Magnetic, Mechanical and Electrical Properties of Ferromagnetic Films, Studied by Automated Wafer Mapping

A number of studies have employed the use of test structures to characterise residual stress and electrical resistivity in NiFe films. However, test structures capable of routine measurement of permeability using standard electrical probing have not been previously reported, and hence neither has the spatial variability of permeability been wafer mapped. The ability to perform this measurement with relatively simple electrical measurements provides an opportunity to provide fast feedback on the magnetic performance of NiFe depositions, which is a capability, required for process control and verification measurements.

Chapter 5 details the development of a test chip, which is capable of routine measurements of electrical resistivity mechanical strain and magnetic permeability. Furthermore, automated wafer mapping has been employed to determine the spatial variation in %Fe composition, NiFe thickness, DC resistance, RF resistance, resistivity, skin depth and permeability at 448 points across the wafer. Optical measurements were taken at 112 points across the 100mm wafer to determine the spatial variation in strain, measured using strain indicator test structures.

The wafer maps produced from measurements on the developed test chip have allowed for successful correlation analysis on electroplated ferromagnetic films to be conducted. Where the lowest correlation coefficient of permeability with %Fe composition was determined to be 0.78. Hence, indicating that a strong correlation was determined. This on-chip characterisation method detailed in this study contrasts with

other magnetic measurements such as the B-H loop, which requires wafers to be diced to create the required small samples.

For the first time this study has demonstrated a method of characterising permeability at high frequency, on wafer. Additionally, the development of a test chip which can characterise and wafer map thickness, composition, electrical resistivity, skin depth, permeability, mechanical strain, resistance at DC and RF will improve upon the existing ability to perform on wafer measurements for process control and verification. Furthermore, the correlation of all of these attributes provides the opportunity to optimise the magnetic core material composition.

7.2.4 Effect of Seed Layer on the Performance of Planar Spiral Microinductors

Chapter 6 has detailed the first characterisation of the effect of seed layer on properties of electroplated NiFe and the performance of planar spiral microinductors, with NiFe cores. This study has determined that replacing the conventional copper seed layer with nickel has made no difference to the composition of the electroplated NiFe, determined by wafer mapping 448 XRF measurements on 100mm wafer. However, the electrical resistivity of NiFe electroplated on Ni seed layers was found to be 9.6% greater than those electroplated on copper. This is to be expected due to the greater electrical resistivity of Ni, and is beneficial for reducing eddy currents in the NiFe core.

Wafer maps of strain measured an average of 18% lower angular deflection when electroplating on copper. However, it is unclear whether this is the result of a stress reduction in the NiFe or result of a reduction in the deflection of the strain indicator structure, due to lower tensile stress in sputtered copper compared to nickel [203, 204].

Additionally, the use of a Ni seed layer measured 2.3% greater magnetic flux density in the NiFe films, than those electroplated on copper. This is to be expected due to the greater volume fraction of magnetic material.

To confirm the effect of seed layer on the performance and efficiency of planar spiral microinductors the test bed inductor process, developed in chapter 3, was used to fabricate inductors with copper and nickel seed layers and a number of patterned magnetic cores. While inductors that incorporate a Ni seed layer consistently produced

greater inductance values and Q-factors than those with copper seed layers, it is clear that the contribution from seed layer is dependent upon the patterning of the magnetic core. Hence, the impact of replacing the conventional copper seed layers with nickel seed layers is the development of more efficient inductors with lower device footprints, and hence more efficient, compact power supply solutions.

7.3 Future Work

The purpose of this thesis has been to develop measurements and structures to characterise materials and processes for evaluating the performance and reliability of fabricated inductors. This having been achieved, there is now the opportunity to optimise the performance of these inductors. As a result of the benchmarking work reported in chapter 6, a number of strategies have been outlined that have the potential to improve the inductor performance of the design/architecture reported in this work. These include fully utilising the device footprint with coils and optimising the electroplating bath setup to improve the permeability of the Permalloy core. It is estimated that incorporating both of these improvements into the type 1 inductor with a Ni seed layer could potentially increase the inductance from 144nH to 6.3μH, using the same device footprint.

Furthermore, as a result of the work presented in this thesis, it has become apparent that the geometry and structure of the magnetic core makes an extremely significant contribution towards device performance. Chapter 6 identified that patterning the inductor's magnetic core with the mesa structures presented in figure 6.5 (f), improves the Q-factor of the device by up to 219%, whilst decreasing the inductance value by 88% (when compared to non-patterned films cores, with type 3 architecture at 10MHz). This provides the basis to move beyond this research and focus on advancing magnetic core technology that can be integrated with silicon IC, with the goal of developing on-chip power solutions including transformers, convertors and power supplies.

While eddy currents cannot be eliminated they can be reduced. Laminating the core, where several thin layers of magnetic material are stacked between thin dielectric layers, effectively increases the core's resistance and reduces the parasitic current. However, current methods of fabricating on-chip laminated cores are complex and

hence not commercially viable due to the need for repeated lithography, seed layer deposition, electroplating and dielectric deposition steps. Three innovative approaches that could optimise both the fabrication and performance of on-chip magnetic core technology are proposed. The first is to develop an electroless lamination deposition method. This removes the need for seed layers and electrical connections, significantly reducing the processing time and cost.

A second activity for improving core efficiency is to split the core into smaller segments, as in figure 6.5 (f and g), which shows mesa structures designed to be 10µm × 30µm spaced 10 µm apart. There is significant opportunity to further improve the efficiency and performance of the core, by significantly reducing the area and gaps between mesa structures. The proposed solution is to aggressively reduce the size of the mesa structures to 1µm x 1 µm (close to the size of an individual magnetic domain) and gap between structures to 1 µm. This will present a significant fabrication challenge as these feature sizes are below what is achievable with conventional contact printing and will require the use of wafer stepper technology.

The final element is based upon the well-known fact that due to the interplay of the intrinsic magnetic energies, the behaviour of magnetic materials patterned at dimensions close to those of individual magnetic domains can be markedly different to that exhibited by continuous films. The magnetic states in patterned segments are defined by the dominant contribution of particular magnetic energies, which arise from the specific size and shape of the segment, as well as from the interactions between neighbouring segments. Using this principal, together with further reductions in dimensions it will be possible to induce uniaxial shape anisotropy in the core, thus further enhancing performance.

7.4 Final Remarks

The work presented in this thesis has characterised materials and processes that can be integrated into a planar spiral microinductor processes to improve reliability, yield and performance of the fabricated device.

The successful characterisation and integration of Parylene with the planar spiral inductor process is expected to improve the reliability of the inductor, when compared to those, which incorporate SU-8. While stress after thermal processing at 140°C

presents similar levels to SU-8, Parylene has presented no issues with adhesion. Additionally, the inductor process that incorporates Parylene lowers the maximum processing temperature of the fabrication process and subsequently residual stress in NiFe layers. Hence, the impact of this work will be an improvement on reliability of the power supply solutions.

For the first time test structures for the on wafer measurement of permeability have been detailed in this thesis. The ability to characterise this property on wafer provides feedback on magnetic material performance that is required for process control and verification measurements. This data combined with wafer mapping characterisation of composition, thickness, resistivity and mechanical strain enables the correlation of these parameters to be quantified, which provide valuable information to support the development of an optimal composition of the electroplated film to be determined. The impact of this work is the improvement of the existing ability to perform on wafer measurements of ferromagnetic materials.

Finally, the performance of planar spiral microinductors has been improved by the replacement of conventional copper seed layers with nickel for the electroplating of NiFe. However, the increase in inductance and Q-factor has been shown to also be the dependent upon how the magnetic core is patterned.

Appendix A
Process Run Sheets

This appendix includes process run sheets for microinductors and test structures fabricated as part of this thesis.

A.1 Test-Bed Planar Spiral Inductor Fabrication Process

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
1.	Deposit SiO_2	Furnace	Wetox 40, 2 hours 40 min			
2.	1st Seed Layer	OPT/Balzers	Ti(30nm)-Cu/Ni(300nm)-Ti(30nm)			
3.	Spin Coat NR2	Polos Spinner	1. Dispense puddle of NR2-20000P 2. 100, 15 sec, 1000 RPM/s 3. 300, 10 sec, 1000 RPM/s 4. 500, 10 sec, 1000 RPM/s 5. 6000, 40 sec, 1000 RPM/s			
4.	Soft Bake	Hotplate (Bay 10)	1. 70°C, 1 min on pins, 20 min contact 2. 140°C, 1 min on pins, 2 min 30 sec contact			
5.	Exposure	Karl Suss	Soft contact, 50 sec			
6.	Post Exposure Bake	Hotplate (Bay 10)	100°C, 1 min on pins, 10 min contact			
7.	Develop	Wet deck (Bay 7)	RD6, dish develop			
8.	Strip Ti layer	Wet deck (Bay 8)	1% HF, 10 sec			
9.	Electroplate NiFe	SMC Tool Copper Bath	10mA/cm^2, approximately 30min			
10.	Strip Resist	Wet Deck (Bay 2)	ACT, approximately 10 min.			
11.	Etch Seed Layer	Wet Deck (bay 8)/JLS	25g/l Ammonium persulphate, 25g/l citric acid in NaOH solution Or Ar Mill, 2 hours (15min run time, 15 min cool)			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
12.	Deposit Parylene	SCS Parylene Tool	5µm Parylene			
13.	CMP	Presi-CMP Tool	Back pressure – 0.4Bar; down force – 0.17Bar; pressure on wafer – 0.25Bar; platen speed – 30RPM; wafer speed – 35RPM, time – 6min.			
14.	2nd Seed Layer	OPT	Ti(30nm)-Cu(100nm)-Ti(30nm			
15.	Spin Coat NR2	Polos Spinner	1.Dispense puddle of NR2-20000P 2. 100, 15 sec, 1000 RPM/s 3. 300, 10 sec, 1000 RPM/s 4. 500, 10 sec, 1000 RPM/s 5. 2000, 40 sec, 1000 RPM/s			
16.	Soft Bake	Hotplate (Bay 10)	6. 70°C, 1 min on pins, 20 min contact 7. 140°C, 1 min on pins, 2 min 30 sec contact			
17.	Exposure	Karl Suss	Soft contact, 150 sec			
18.	Post Exposure Bake	Hotplate (Bay 10)	100°C, 1 min on pins, 10 min contact			
19.	Develop	Wet deck (Bay 7)	RD6, dish develop			
20.	Electroplate copper	SMC Tool Copper Bath	10mA/cm^2, approximately 1 hour 10 min			
21.	Strip Resist	Wet Deck (Bay 2)	ACT, approximately 10 min.			
22.	Etch Seed Layer	Wet Deck (bay 8)	1% HF for Ti layers 25g/l Ammonium persulphate, 25g/l citric acid in NaOH solution for Cu layers			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
23.	Deposit Parylene	SCS Parylene Tool	5µm parylene			
24.	Deposit Ti	OPT	Ti(30nm)			
25.	Spin Coat NR2	Polos Spinner	1. Dispense puddle of NR2-20000P 2. 100, 15 sec, 1000 RPM/s 3. 300, 10 sec, 1000 RPM/s 4. 500, 10 sec, 1000 RPM/s 5. 2000, 40 sec, 1000 RPM/s			
26.	Soft Bake	Hotplate (Bay 10)	1. 70°C, 1 min on pins, 20 min contact 2. 140°C, 1 min on pins, 2 min 30 sec contact			
27.	Exposure	Karl Suss	Soft contact, 150 sec			
28.	Post Exposure Bake	Hotplate (Bay 10)	100°C, 1 min on pins, 10 min contact			
29.	Developer	RD6 Polos Spinner	Program 3			
30.	Ti Etch	Wet Deck (Bay 8)	1% HF, approximately 10sec			
31.	Etch Parylene	JLS	Parylene etch, approximately 1 hour 30 min			
32.	Strip Resist	Wet Deck (Bay 2)	ACT, approximately 10 min.			
33.	Ti Etch	Wet Deck (Bay 8)	1% HF, approximately 10sec			
34.	CMP of parylene	Presi-CMP Tool	Back pressure – 0.4Bar; down force – 0.17Bar; pressure on wafer – 0.25Bar; platen speed – 30RPM; wafer speed – 35RPM, time – 6min.			
35.	Deposit Parylene	SCS Parylene Tool				

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
36.	Deposit Ti	OPT	Ti Deposition (30nm)			
37.	Spin Coat NR2	Polos Spinner	1. Dispense puddle of NR2-20000P 2. 100, 15 sec, 1000 RPM/s 3. 300, 10 sec, 1000 RPM/s 4. 500, 10 sec, 1000 RPM/s 5. 2000, 40 sec, 1000 RPM/s			
38.	Soft Bake	Hotplate (Bay 10)	1. 70°C, 1 min on pins, 20 min contact 2. 140°C, 1 min on pins, 2 min 30 sec contact			
39.	Exposure	Karl Suss	Soft contact, 97 sec			
40.	Post Exposure Bake	Hotplate (Bay 10)	100°C, 1 min on pins, 10 min contact			
41.	Developer	RD6 Polos Spinner	Program 3			
42.	Ti Etch	Wet Deck (Bay 8)	1% HF, approximately 10sec			
43.	Etch Parylene	JLS	Parylene etch, approximately 1 hour 30 min			
44.	Strip Resist	Wet Deck (Bay 2)	ACT, approximately 3 min.			
45.	Ti Etch	Wet Deck (Bay 8)	1% HF, approximately 10sec			
46.	3st Seed Layer	OPT/Balzer	Ti(30nm)-Cu(300nm)-Ti(30nm)/Ti(30nm)-Ni(300nm)-Ti(30nm)			
47.	Spin Coat NR2	Polos Spinner	1. Dispense puddle of NR2-20000P 2. 100, 15 sec, 1000 RPM/s 3. 300, 10 sec, 1000 RPM/s 4. 500, 10 sec, 1000 RPM/s 5. 2000, 40 sec, 1000 RPM/s			
48.	Soft Bake	Hotplate (Bay 10)	1. 70°C, 1 min on pins, 20 min contact 2. 140°C, 1 min on pins, 2 min 30 sec contact			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
49.	Exposure	Karl Suss	Soft contact, 93 sec			
50.	Post Exposure Bake	Hotplate (Bay 10)	100°C, 1 min on pins, 10 min contact			
51.	Developer	RD6 Polos Spinner	Program 3			
52.	Ti Etch	Wet Deck (Bay 8)	1% HF, approximately 10sec			
53.	Electroplate NiFe	SMC Plating Tool	10mA/cm^2, approximately 30 min			
54.	Remove Seed Layer	JLS	25g/l Ammonium persulphate, 25g/l citric acid in NaOH solution Or Ar mill, 2 hours			

A.2 Parylene Strain Indicator Test Structure Fabrication Process

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
1.	Polysilicon Deposition	Furness	Wet ox			
2.	Deposit Parylene	SCS Parylene Tool	5µm Parylene (approx. 5.5g dimer)			
3.	SPR 220-7 surface treatment	Primer Dep	HMDS primer, expose to vapour at room temperature for 10 min			
4.	Spin coat 7µm thick SPR 220-7	NR2 spinner, with bowl liners	1. 700 RPM, 10 sec, 1000RPM/sec 2. 3000 RPM, 60 sec, 1000RPM/sec			
5.	Soft bake	Hot plate	1. 115˚C, 60 sec on pins, 90 sec contact. 2. Allow 90 sec for wafer to cool			
6.	Exposure	Karl Suss MA8	Soft contact, 50 sec			
7.	Develop	Wet deck	MF-26A dish develop, approximately 1 min			
8.	Etch Parylene	JLS RIE 80	Parylene etch, approximately 50min			
9.	Strip Resist	Wet Deck	Acetone, 1 min			
10.	Thermal Treatment	Hot plate	Wafer 1: no thermal treatment Wafer 2: 70˚C, 1 min pins, 15 min contact Wafer 3: 140˚C 1 min pins, 15 min contact Wafer 4: 200˚C 1 min pins, 15 min contact			
11.	Strain indicator structure release	MEMStar XeF_2	SU-8/Parylene strain indicator structure release etch			

A.3 SU-8 5 Strain Indicator Test Structure Fabrication Process

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
12.	Polysilicon Deposition	Furness	Wet ox			
13.	SU-8 Substrate Preparation (Wafer Cleaning)	Wet Decks	3:1 Piranha etch, 5 min			
14.	SU-8 Substrate Preparation (Wafer Cleaning)	Barrel Asher	30 min			
15.	SU-8 Substrate Preparation (dehydration)	Hot plate	200ºC, 2 min			
16.	Coat SU-8 3005	Polos Spinner	5 µm thickness (process 50 on spinner) 3. Dispense puddle of SU-8 3005 4. 100 RPM, 15 sec, 1000RPM/sec 5. 300 RPM, 10 sec, 1000RPM/sec 6. 500 RPM, 5 sec, 1000RPM/sec 7. 3000 RPM, 30 sec, 1000 RPM/sec			
17.	Soft Bake	Hot Plate	3. 65ºC, 1 min on pins, 1 min contact 4. 95ºC, 1 min on pins, 3 min contact 5. 65ºC, 1 min on pins, 1 min contact			
18.	Exposure	Karl Suss	Spacers/Proximity, approximately 15 sec exposure (calibrate exposure time)			
19.	Post Exposure Bake	Hotplate	1. 65ºC, 1 min on pins, 1 min contact 2. 95ºC, 1 min on pins, 2 min contact 3. 65ºC, 1 min contact, 1 min on pins			
20.	Develop	Wet Deck	PGMEA, approximately 1 min, rinse with IPA			
21.	Hard Bake	Hotplate	1. 200ºC, 1 min on pins, 15 min contact OR 1. 150ºC, 1 min on pins, 15 min contact OR 1. ramp temperature to 200ºC			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
			2. 200°C, 15 min contact 3. gradually cool down			
22.	Strain indicator structure release	MEMStar XeF_2	SU-8/Parylene strain indicator structure release etch			

A.4 SU-8 3005 Strain Indicator Test Structure Fabrication Process

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
23.	Polysilicon Deposition	Furness	Wet ox			
24.	SU-8 Substrate Preparation (Wafer Cleaning)	Wet Decks	3:1 Piranha etch, 5 min			
25.	SU-8 Substrate Preparation (Wafer Cleaning)	Barrel Asher	30 min			
26.	SU-8 Substrate Preparation (dehydration)	Hot plate	200°C, 2 min			
27.	Coat SU-8 3005	Polos Spinner	5 µm thickness (process 50 on spinner) 1. Dispense puddle of SU-8 3005 2. 100 RPM, 15 sec, 1000RPM/sec 3. 300 RPM, 10 sec, 1000RPM/sec 4. 500 RPM, 5 sec, 1000RPM/sec 5. 4000 RPM, 30 sec, 1000 RPM/sec			
28.	Soft Bake	Hot Plate	1. 65°C, 1 min on pins, 1 min contact 2. 95°C, 1 min on pins, 3 min contact 3. 65°C, 1 min on pins, 1 min contact			
29.	Exposure	Karl Suss	Spacers/Proximity, approximately 15 sec exposure (calibrate exposure time)			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
30.	Post Exposure Bake	Hotplate	1. 65°C, 1 min on pins, 1 min contact 2. 95°C, 1 min on pins, 2 min contact 3. 65°C, 1 min contact, 1 min on pins			
31.	Develop	Wet Deck	PGMEA, approximately 1 min, rinse with IPA			
32.	Hard Bake	Hotplate	1. 200°C, 1 min on pins, 15 min contact OR 1. 150°C, 1 min on pins, 15 min contact OR 1. ramp temperature to 200°C 2. 200°C, 15 min contact 3. gradually cool down			
33.	Strain indicator structure release	MEMStar XeF_2	SU-8/Parylene strain indicator structure release etch			

A.5 NiFe Test Chip Fabrication Process

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
34.	Deposit SiO_2	PECVD	700nm LFSIO, approximately 16 min dep			
35.	Ti-Ni-Ti dep	Balzers	Ti(30nm)-Ni(300nm)-Ti(30nm) blanket seed			
36.	Spin coat 7µm thick SPR 220-7	NR2 spinner, with bowl liners	1. 700 RPM, 10 sec, 1000RPM/sec 2. 900 RPM, 60 sec, 1000RPM/sec			
37.	Soft bake	Hot plate	3. 115˚C, 60 sec on pins, 180 sec contact. Allow 90 sec for wafer to cool			
38.	Exposure	Karl Suss MA8	Soft contact, 110 sec			
39.	Develop	Wet deck	MF-26A dish develop, approximately 3 min			
40.	Etch Ti	Wet deck	1%HF bath, approximately 10 sec			
41.	Electroplate	NiFe electroplating bath	10mA/cm^2 approximately 1 hour 40 min			
42.	Strip SPR 220-7	Wet deck	Acetone strip, approximately 2 min			

Step	Description	Equipment	Recipe/Parameters	Date	Operator	Comments
43.	Etch seed layer	Wet deck	1. 1%HF bath, approximately 10 sec 2. Ar mill 3. 1%HF bath, approximately 10 sec			
44.	Electrical measurements		Conduct composition, thickness, DC and RF resistance measurements			
45.	Strain indicator structure release	MEMStar HF tool	NiFe strain indicator structure release etch			

Appendix B
Enlarged Wafer Maps

This appendix includes enlarged wafer maps from Chapters 4 and 5.

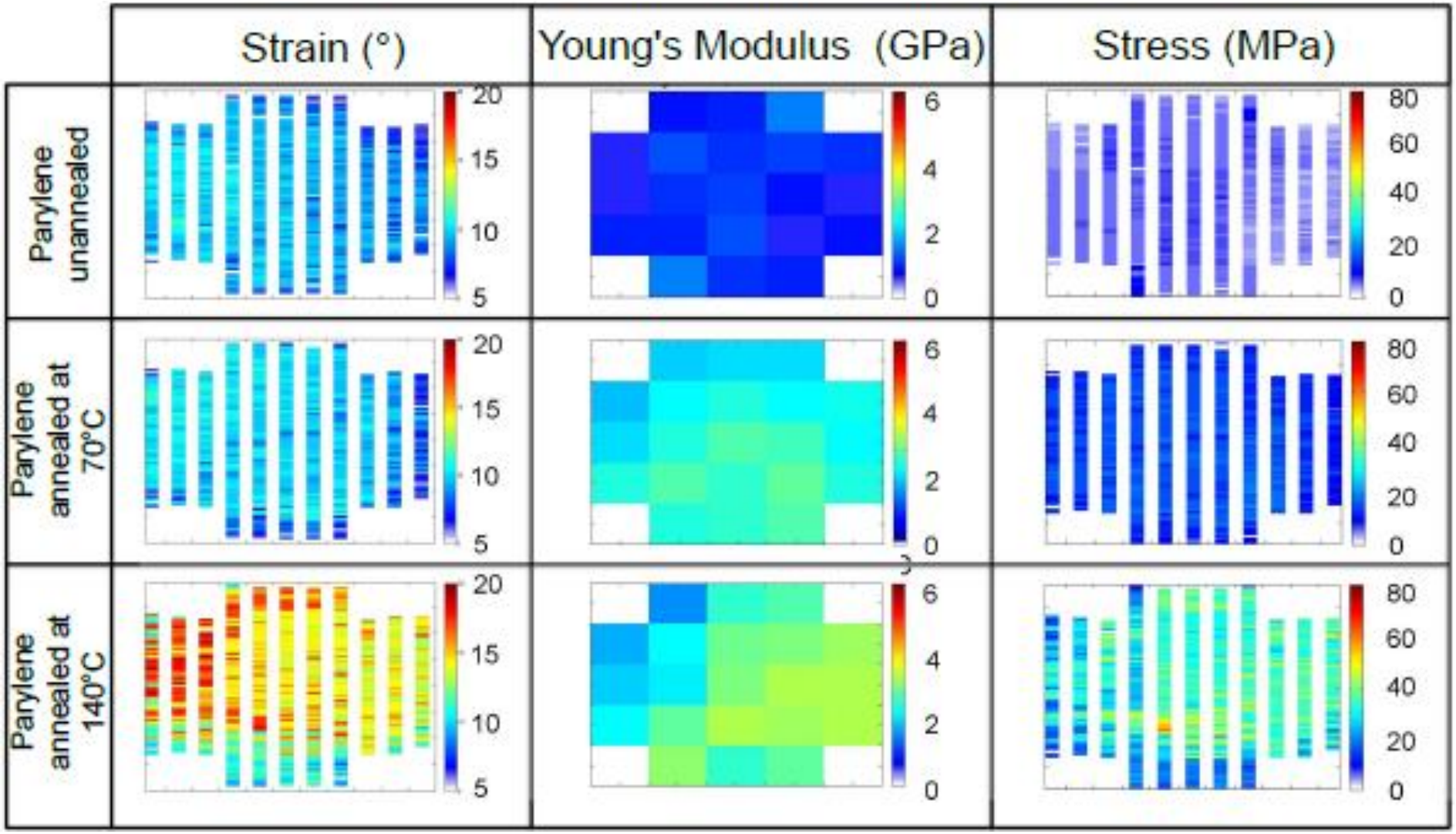


Figure B.1: *Wafer maps of Parylene strain, Young's modulus and Stress for films with different thermal histories.*

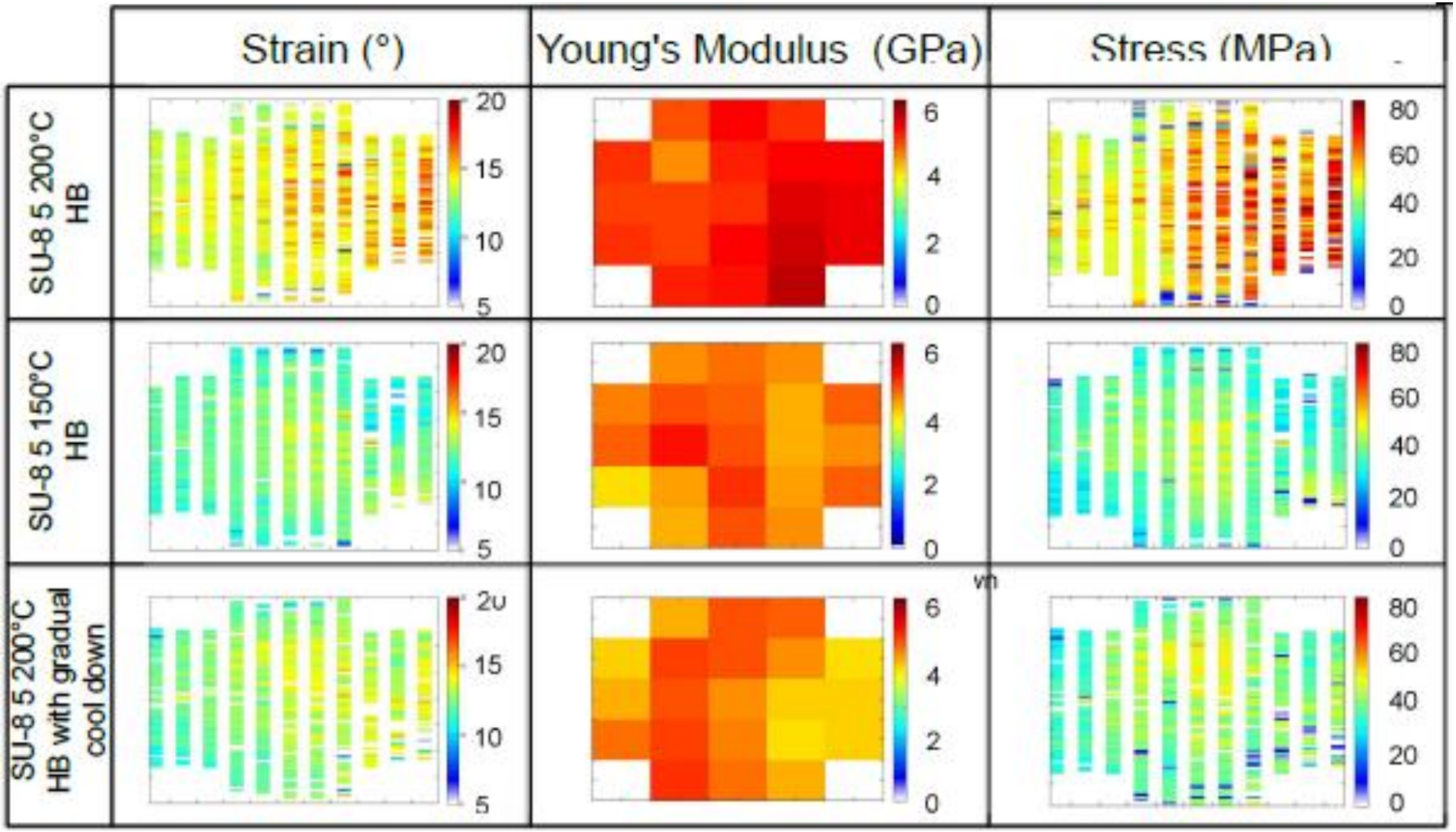


Figure B.2: *Wafer maps of SU-8 5 strain, Young's modulus and Stress where the hard-bake parameters have been varied for each film.*

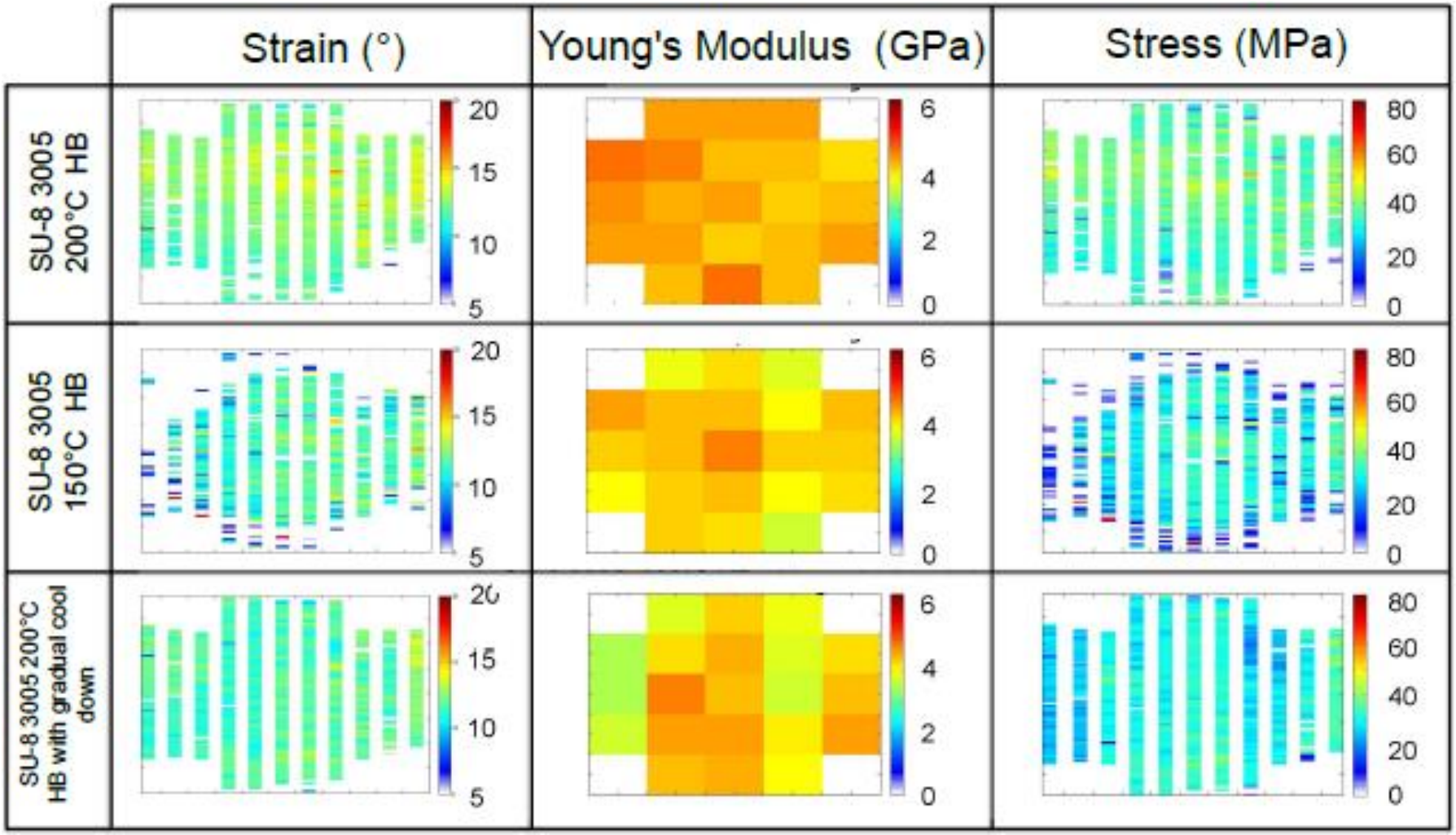


Figure B.3: *Wafer maps of SU-8 3005 strain, Young's modulus and Stress where the hard-bake parameters have been varied for each film.*

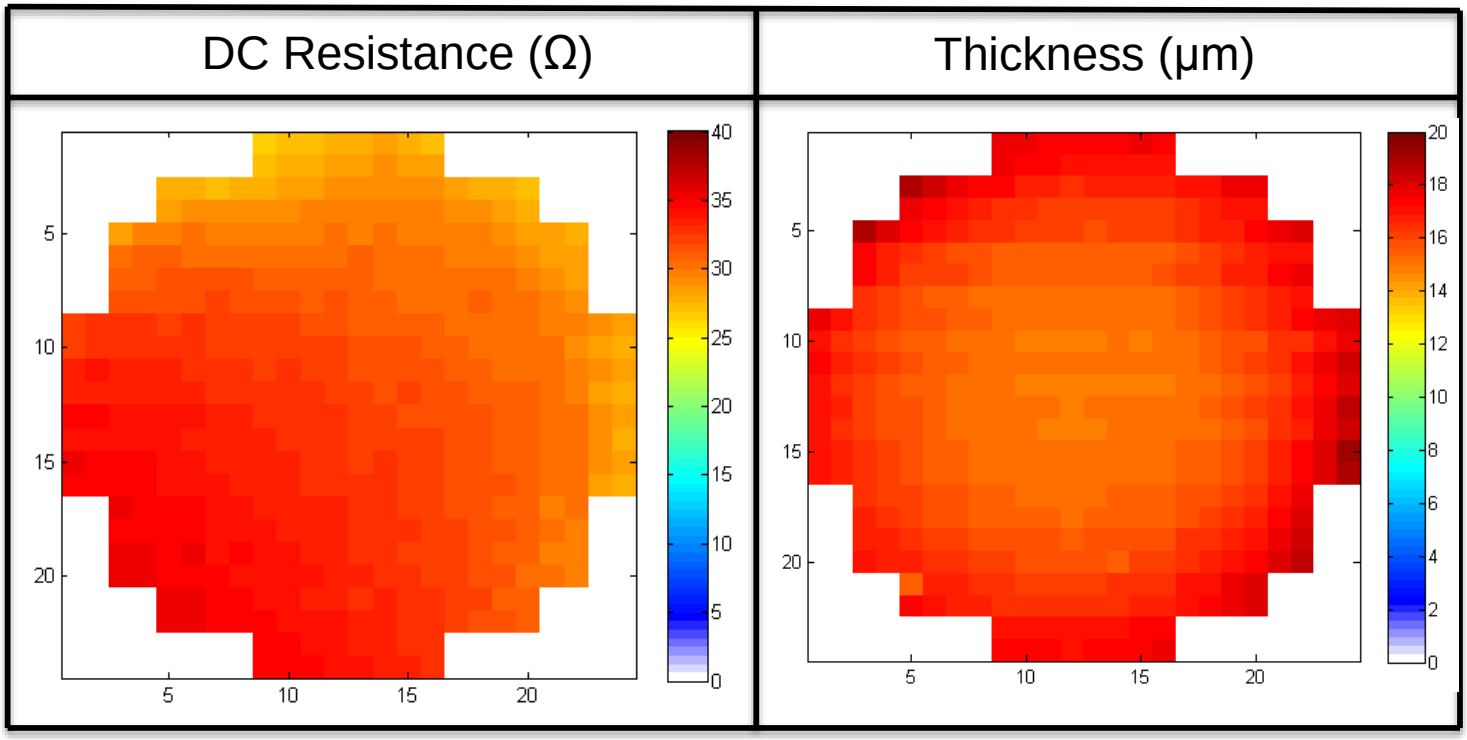


Figure B.4: *Wafer maps of thickness and composition wafer maps of electroplated NiFe films.*

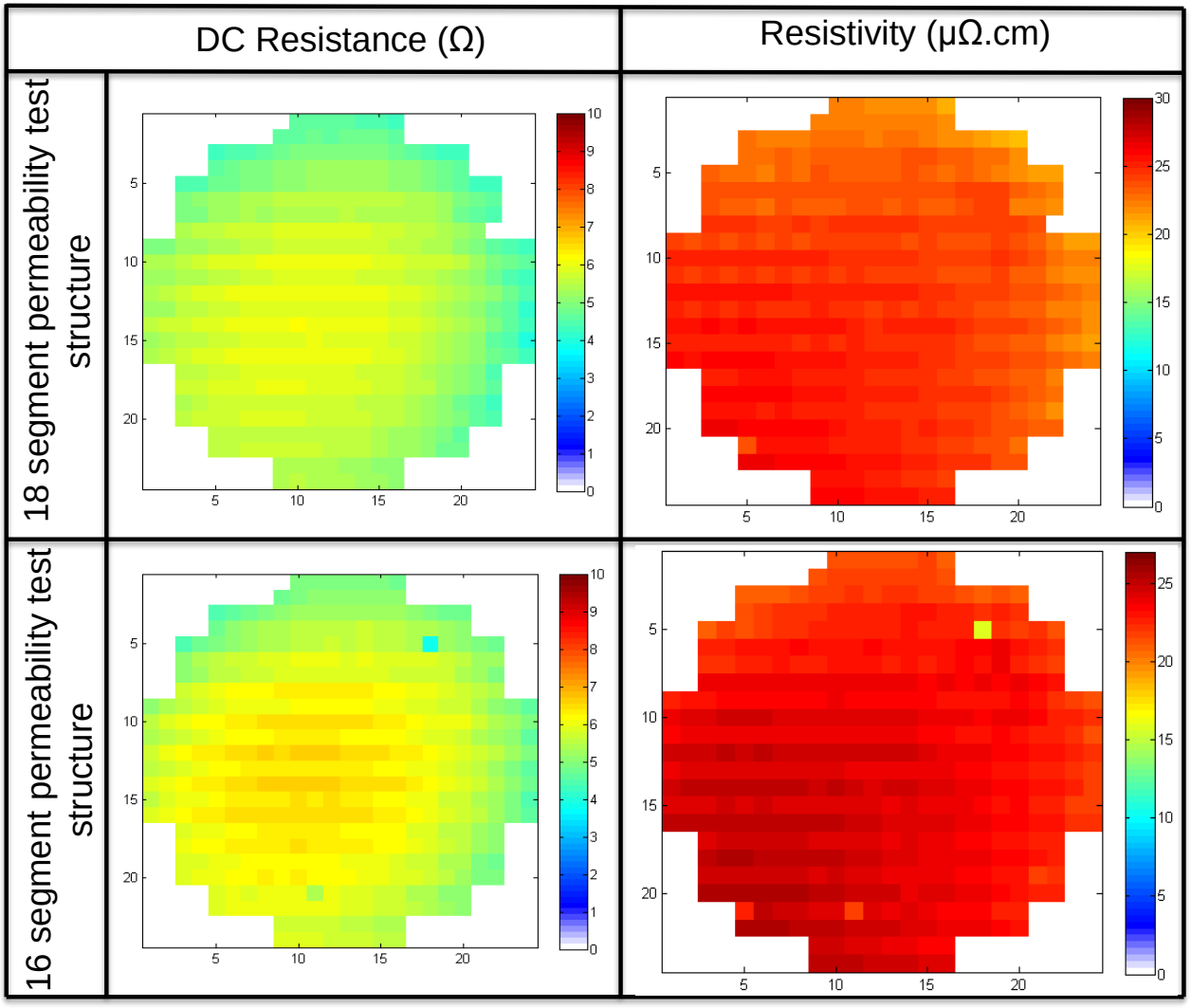


Figure B.5: *Wafer maps DC resistance and resistivity for the 18 and 16 segment NiFe permeability test structures.*

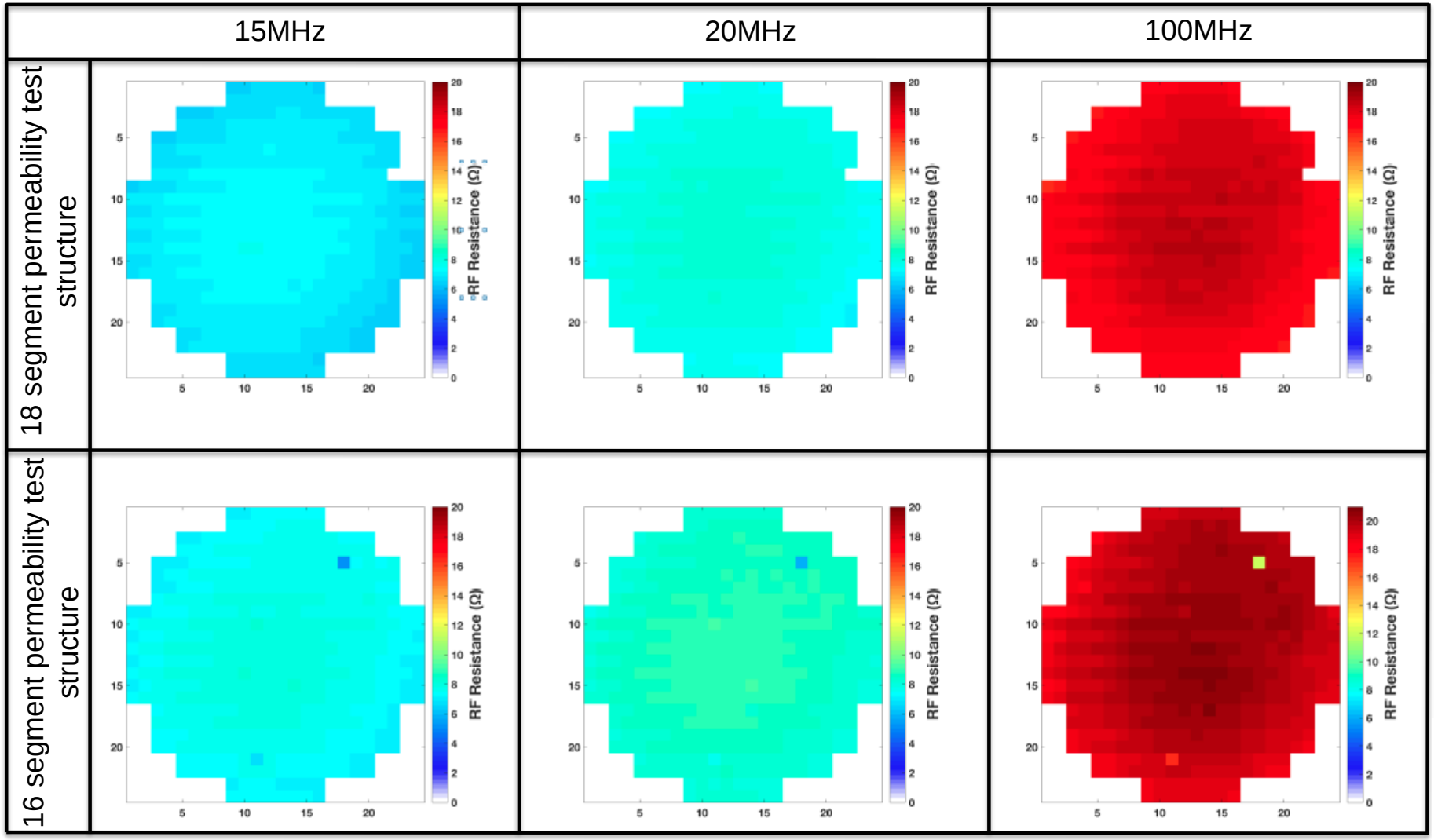


Figure B.6: *Wafer maps of RF resistance for the 18 and 16 segment NiFe permeability test structures.*

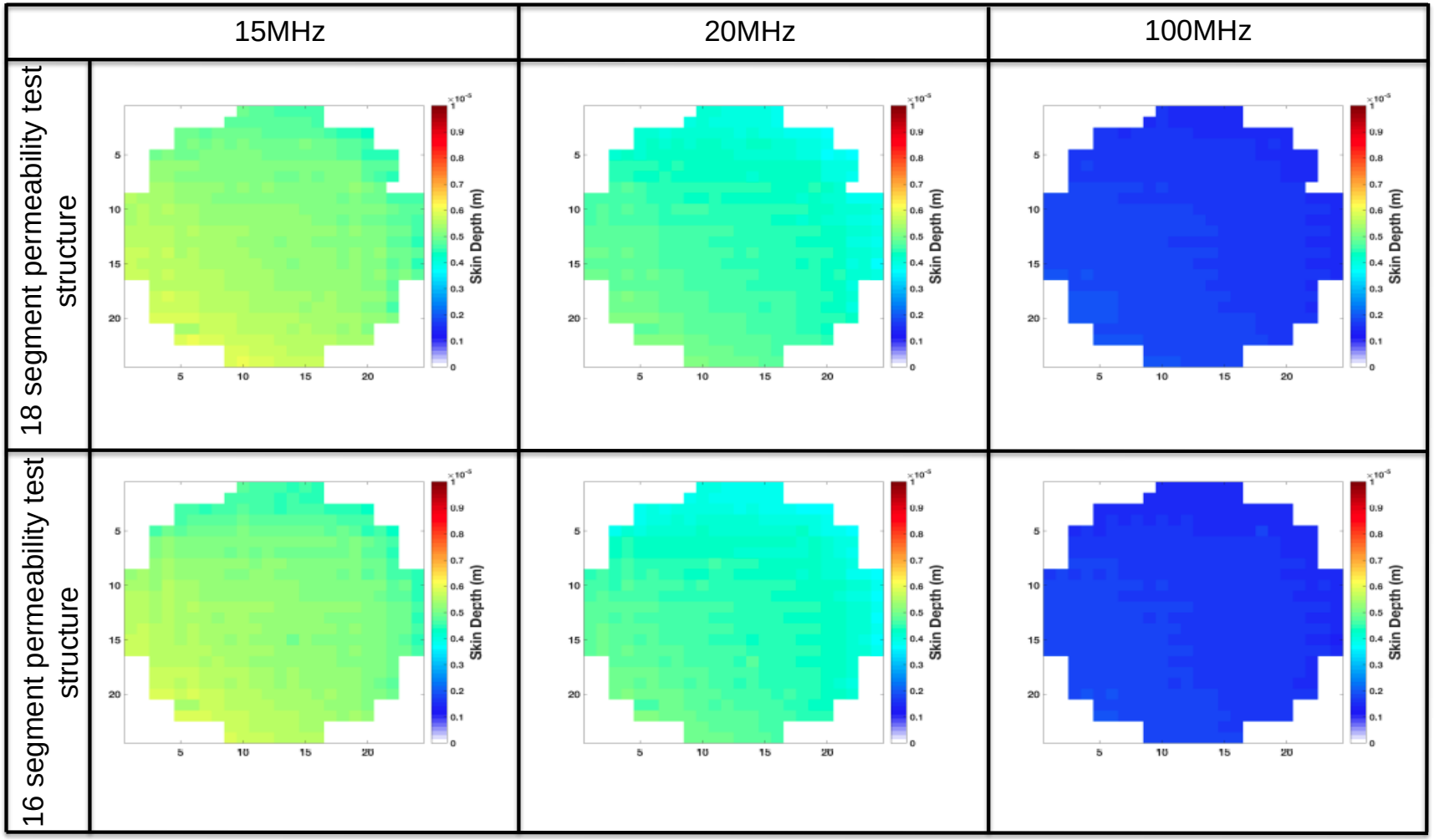


Figure B.7: *Wafer maps of skin depth for the 18 and 16 segment NiFe permeability test structures.*

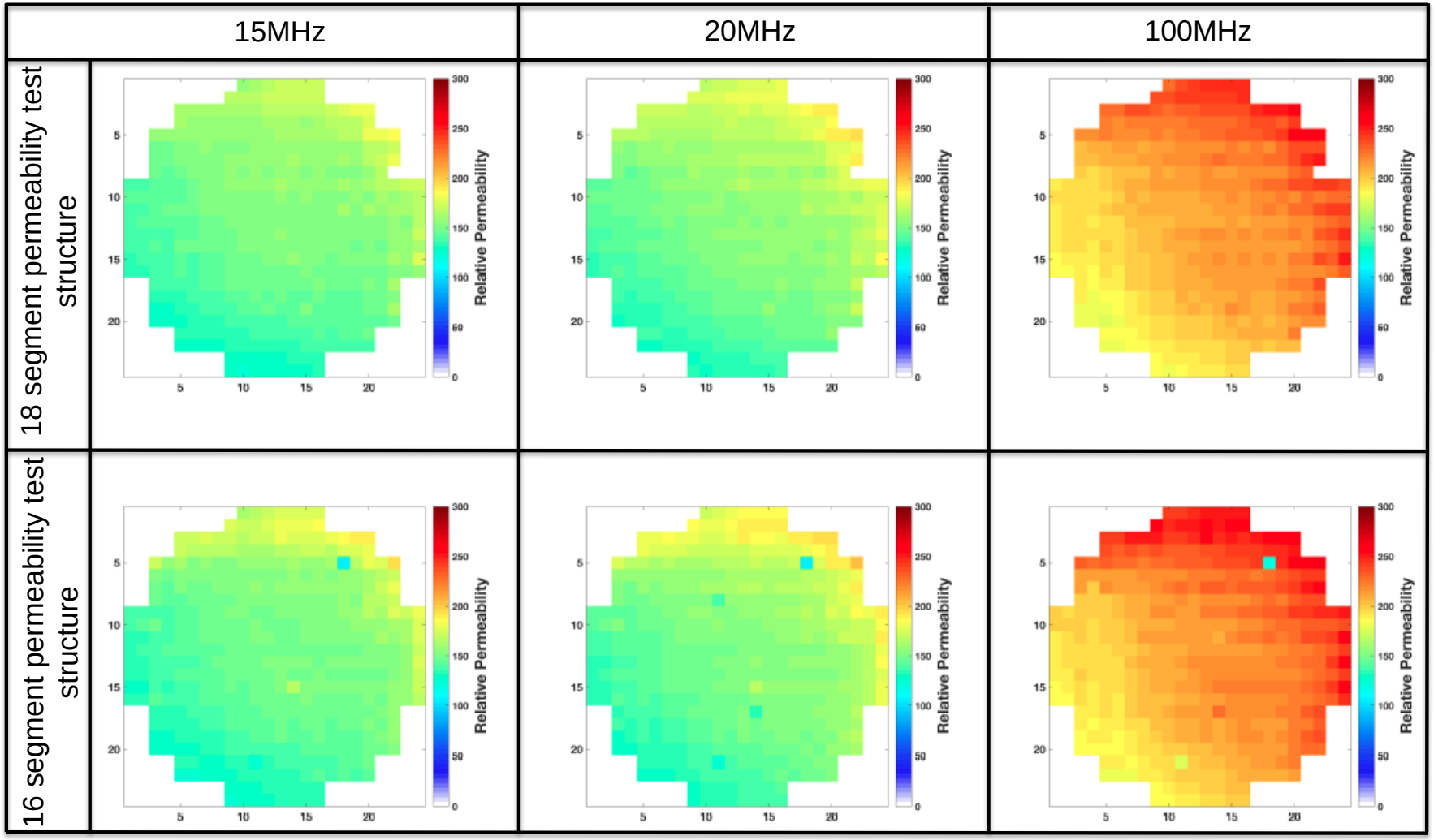


Figure B.8: *Wafer maps of relative permeability for the 18 and 16 segment NiFe permeability test structures.*

Appendix C
Correlation of Measurements from NiFe Test Chip

This appendix details graphs off all measured data points measured from the NiFe test chip reported in Chapter 5.

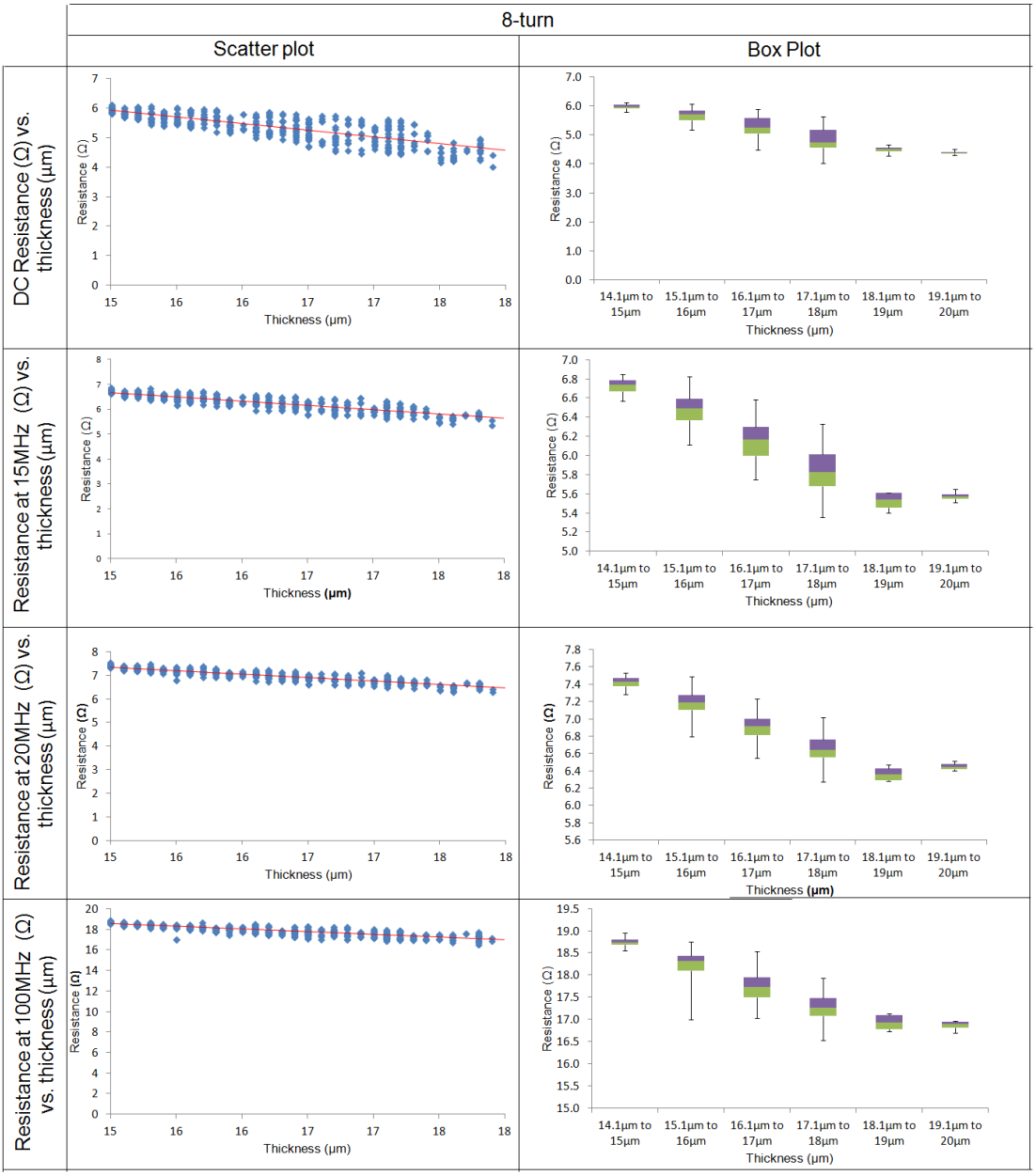


Figure C.1: *Scatter and box plots of resistance at DC, 15MHz, 20MHz, 100MHz against thickness, for 8 turn permeability test structures.*

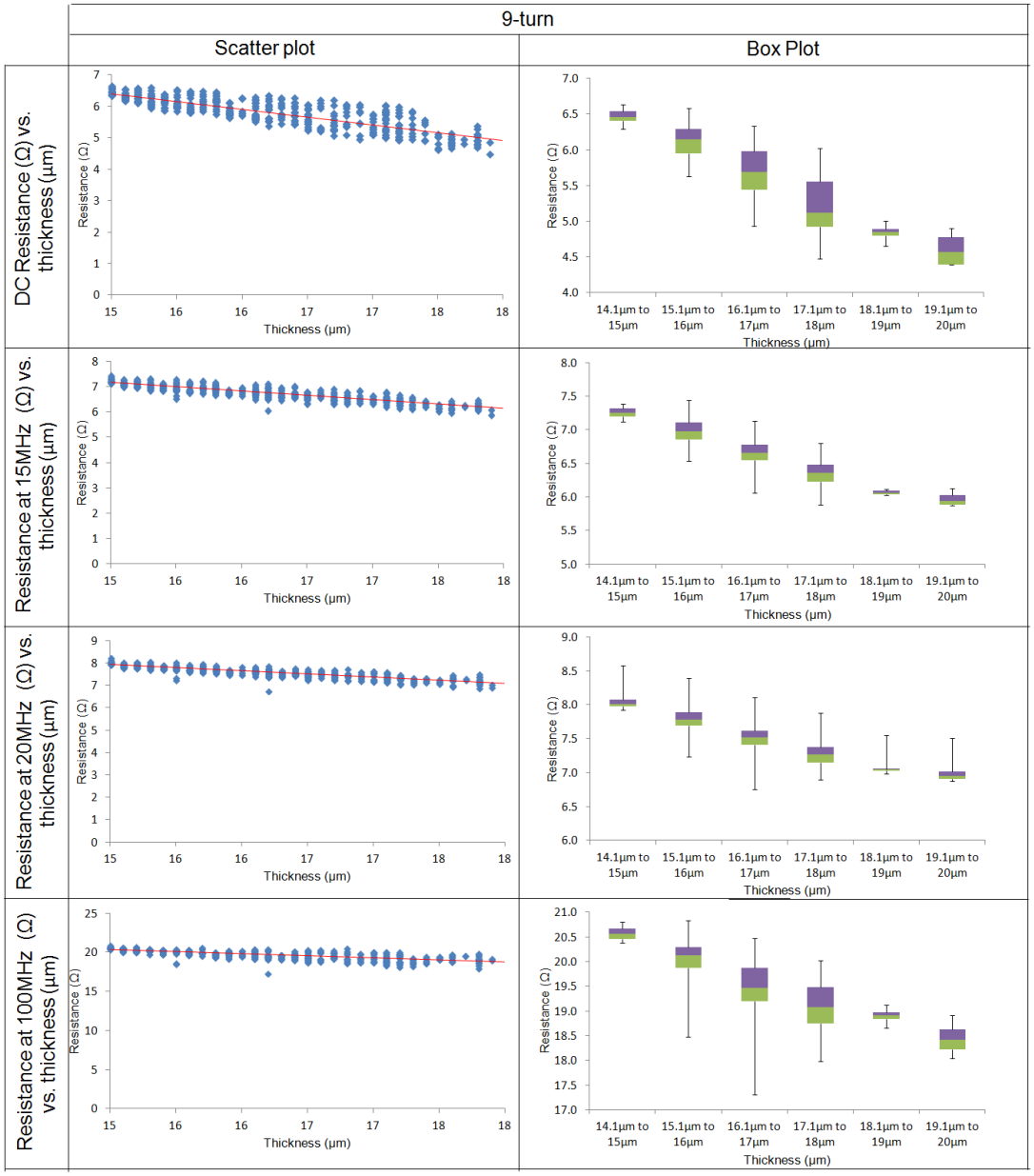


Figure C.2: *Scatter and box plots of resistance at DC, 15MHz, 20MHz, 100MHz against thickness, for 9 turn permeability test structures.*

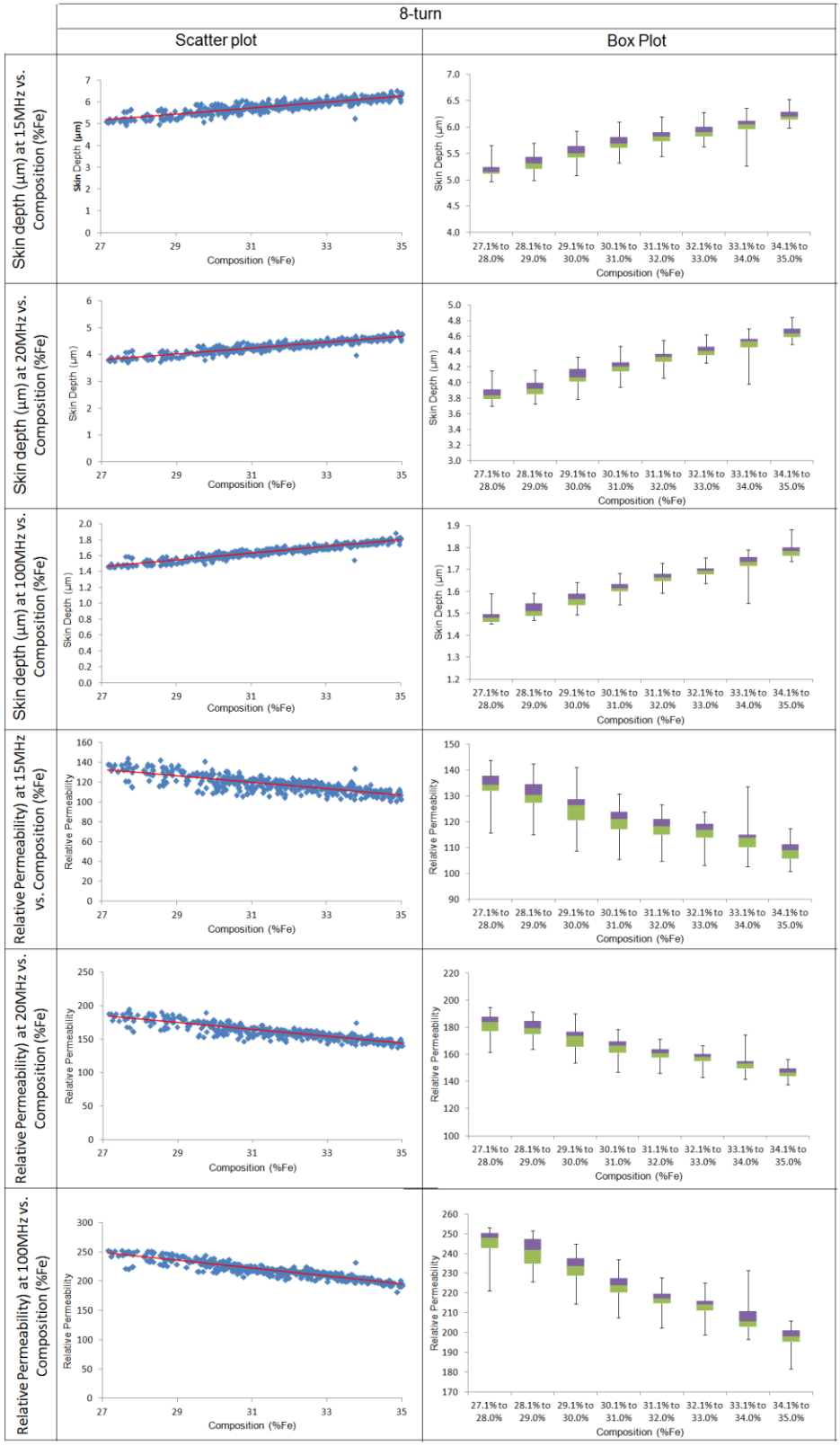


Figure C.3: *Scatter and box plots of resistance at skin depth and permeability at 15, 20 and 100MHz against thickness, for 8 turn permeability test structures.*

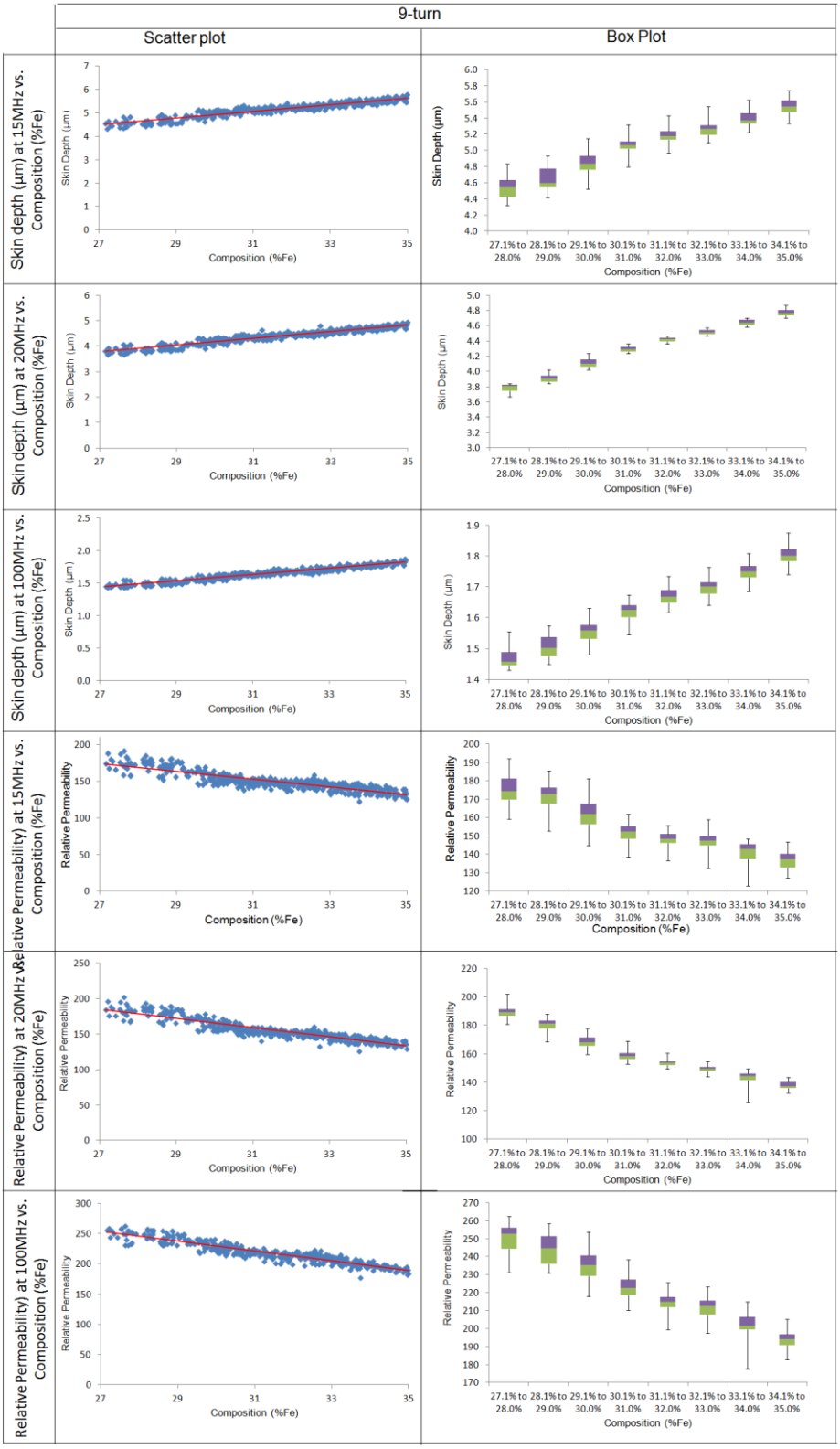


Figure C.4: *Scatter and box plots of resistance at skin depth and permeability at 15, 20 and 100MHz against thickness, for 8 turn permeability test structures.*

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